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New paradigms for advances in efficiency and stability of CdTe solar cells

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New paradigms for advances in efficiency and stability of CdTe solar cells
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Faber est suae quisque fortunae
(Pseudo Sallustio, Epistulae ad Caesarem Senem de re publica, I, I, 2)

Contents

1
Introduction: the reasons of renewable energies

It is no longer possible to deny the existence of climate change: people from every country on every continent are experiencing its significant impacts, which include changing weather patterns, rising sea level, and more extreme weather events.
The consensus of scientific opinion is that the Earth's climate change is being affected by human activity [1]. Since the pre-industrial era, anthropogenic greenhouse gas (GHG) emissions have increased, enhancing the atmospheric concentration of carbon dioxide (CO_2), methane (CH_4) and nitrous oxide (N_2O) to a level that is unprecedented in at least the last 800000 years [1]. This has caused the increase of the natural greenhouse effect, leading to global warming.
Anthropogenic GHG emissions have continued to increase since 1970, driven by the emissions of CO_2 from fossil fuel combustion and industrial processes, which represent about 78% of the total [1].

The Intergovernmental Panel on Climate Change detected some alterations in the environment [1]:

- From 1880 to 2012 the average global temperature increased by 0.85°C;
- From 1901 to 2010, because of the ice melting, the global average sea level rose by 19 cm;
- Since 1979, 1.07 million Km^2 of Arctic ice are lost every decade.

Moreover, it is expected that:

- The world's oceans will warm, and ice melting will continue;
- The average rise in the sea level will be 24-30 cm by 2065, and 40-63 cm by 2100;
- Most aspects of climate change will persist for many centuries even if emissions are stopped.

To face this real emergency, during the 2015 United Nations Climate Change Conference (COP 21) held in Paris, the Paris Agreement was negotiated. For the first time in history this agreement brings all the nations together (the representatives of 196 parties participated in it) for a common cause to undertake ambitious efforts to oppose the climate change. The purpose of this agreement is to keep the global temperature rise below 2 degrees Celsius compared to pre-industrial levels in this century, and to work further to limit the temperature increase to 1.5 degrees Celsius. Moreover, it aims to improve the ability of all countries to deal with the impacts of climate change. To reach these ambitious goals, all countries must do their best to reduce their emissions; they also have to report regularly about their developments [2].

As already mentioned, fossil fuel consumption is the main source of GHG emissions. To reduce them, while maintaining sustainable economic and social development, a real energy revolution is needed.
The transformation of the energy system requires [3]:

- To avoid wasting energy and to improve technologies to use them more efficiently; thus, reducing the energy demand growth;
- To develop renewable energies, increasing their impact to the detriment of fossil energy.

A low-carbon energy system dominated by renewable energy should replace the high-carbon energy system dominated by fossil energy; in that way a near-zero CO_2 emission system will be achieved [3].

Moreover, another aspect to underline is that fossil fuels are destined to be finished quickly, because their consumption rate is enormously higher than the production one.
Renewable are those sources whose current use does not affect their availability in the future; thus, solar, hydroelectric, wind, marine, geothermal and biomass energy. The solution of the energy problem will not be a single source, but the combination of all these, each one used where it is appropriate.
Nuclear energy was not mentioned among renewables, since it is based on the utilization of limited combustible reserves of mineral origin. Anyway, this source could contribute to the CO_2 emission reduction, though it presents other problems such as the risk of nuclear accidents and the production of radioactive waste.

The massive use of fossil fuels started at the end of the XVIII century, when the steam engine invented by James Watt, powered by coal, began the first industrial revolution. At the end of the XIX century oil was discovered, and in few years it began to compete with coal, overcoming it by the early 1960s. Decades of cheap fossil fuels helped the economic boom after the second world war [4]. In that time renewable energies were already known and studied, but there was not a real need, or rather, a real intention to replace fossil fuels. As a matter of fact, traditional sources could be efficiently stored, they were accessible, which means they could be used where and when it was necessary, and they had a higher energy density which means that a larger amount of energy could be produced with a lower amount of substance. Basically, they were cheap and convenient.

Regarding the solar energy case, as early as in 1954 researchers at Bell Laboratory (Murray Hill, New Jersey) demonstrated their solar panel by using it to power a small toy Ferris wheel and a solar powered radio transmitter. Those first silicon solar cells had a 6 % efficiency at converting the energy of sunlight into electricity; a huge improvement over any previous solar cells [5]. They patented them the following year, but the solar cells were expensive to produce, and the first efforts at commercializing the invention did not have much success. Within a few years solar cells were developed for space applications and commonly used to power satellites, but the domestic use was not really considered [6].
In 1973 the “first oil shock” also called the “1973 oil crisis” happened. In the same year Arab-Israeli War, the Arab members of the Organization of Petroleum Exporting Countries (OPEC) imposed an embargo both against United States, which supplied the Israeli military,

and other countries that supported Israel such as Canada, Japan, the Netherlands, the United Kingdom, Portugal, Rhodesia and South Africa. This embargo interrupted petroleum exports to these states and introduced cuts in the production. By the end of the embargo in 1974, the price of oil per barrel had quadrupled, leading to huge price increase on consumers, and uncertainty about the stability of national economies [7].
It was probably from this moment on that oil stopped to be seen as the more convenient and always available energy source, and that the real need to find alternatives arose.
Moreover, in November 1974 the International Energy Agency (IEA, founded by 17 countries) was established to implement an international energy program. Its primary mandate was to promote energy security among its member countries through the reduction of excessive dependence on oil, this to be achieved through energy conservation, development of alternative energy sources and energy research and development. These alternative energy sources were natural gas, nuclear energy, but also renewable energies [8].
The response to the "1973 oil shock" probably gave the planet a life-saving head start in the struggle to avoid catastrophic climate change. Politic and economic reasons began what today must be pursued, also and above all, for environmental reasons.

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2
Photovoltaic energy

2.1 The second generation photovoltaic solar cells

Focusing on photovoltaic energy, solar cells, or more precisely photovoltaic (PV) cells, convert sunlight directly into electricity. The name is given by the PV effect, the process of converting light (photons) to electricity (voltage), observed for the first time in 1839 by Alexandre-Edmond Becquerel. Then in 1954 the scientists of the Bell Laboratory (Murray Hill, New Jersey) developed the first practical silicon solar cell [1].
Photovoltaic technologies are generally divided into three generations: devices that exploit the properties of mono or poly crystalline silicon, which for historical reasons is the most diffuse inorganic semiconductor, are included in the first.
The second generation concerns thin film technology, such as solar cells based on amorphous silicon, Cadmium Telluride (CdTe), and Copper Indium Gallium Selenide (CIGS).
Finally, the third generation is based on innovative concepts, covering today a myriad of different type of technologies such as multi junction solar cells, concentrator photovoltaics, organic, polymer, perovskite and quantum dot solar cells.

The photovoltaic market has always been dominated by the first generation. In 2017 it covered 93% of the annual Gigawatt-Peak (GWP) production, mainly because silicon has been studied for many more years, while thin film technology covered 4.5%. CdTe solar cells are the second most common PV technology in the world marketplace after crystalline silicon, and in 2017 they represented 2.3% of the GWP production [2].
The second PV generation has been developed to produce cheaper panels than the ones of the first generation, making use of alternative semiconductors. Indeed, for silicon production high temperatures and long production time are needed. Moreover the requirement to work in complete absence of oxygen and the complexity of cutting and assembly silicon wafers make this technology intrinsically complicated and expensive. Thin film devices can be fabricated with new methods, considerably reducing production costs.
Thin film means a layer of thickness between few tens of angstroms and some microns deposited on a supporting substrate. The deposition of multiple thin layers on a polymeric, glass or metallic substrate creates the thin film technology. For this reason, a smaller amount of semiconductor material is needed (at least a hundred times less). Moreover, since the layers can be deposited straight on a large substrate, these devices are more suitable for large scale production than the first generation ones: the fabrication process is simpler and needs less energy. While crystalline silicon cells are assembled to constitute a panel, thin film cells are obtained from the layers through laser cut; in that way a single production line is needed, and the production is faster [3].
As shown in figure 2.1, mono-crystalline silicon solar cells still have a higher conversion efficiency of 26.7%, but few steps have been made in the last twenty years, while CdTe solar cells have considerably improved reaching 22.1 % efficiency in 2016 [4].

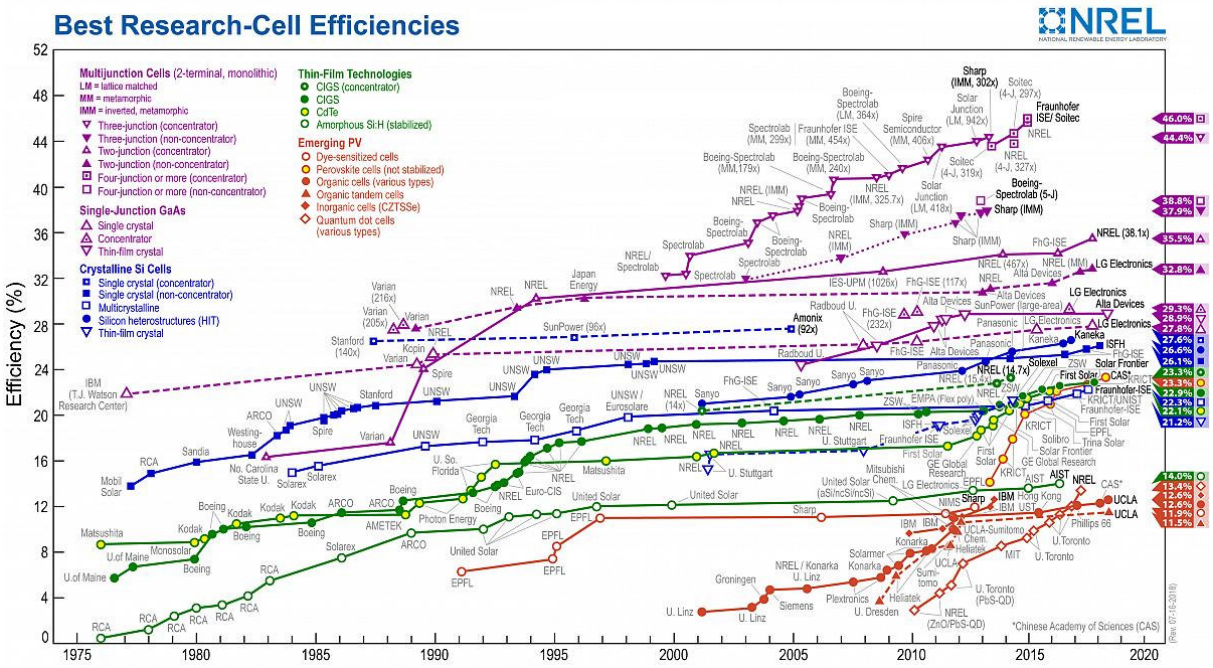

Figure 2.1: NREL efficiency chart of the main solar cells technologies, updated July 2018 [4].

2.1.1 Polycrystalline thin films

CdTe and CIGS are the main semiconductors utilized as polycrystalline thin films. The polycrystalline film is formed by aggregate grains, which are little mono-crystals. The interface between two grains is called grain boundary, and it is a defect because it is a zone where the lattice order is missing. CdTe and CIGS coupled with Cadmium Sulfide (CdS) make the polycrystalline solar cells, which are heterojunctions as formed by different semiconductors.

In order to form an efficient heterojunction, the semiconductors need to have similar electron affinity, lattice parameter and coefficient of thermal expansion, and both must have low resistivity.

To promote cell efficiency, n-type semiconductor must behave as window layer, with a band gap higher than 2 eV, while the p-type must act as absorber, with a band gap around 1.4 eV, which corresponds to the maximum theoretical efficiency for photovoltaic conversion [5].

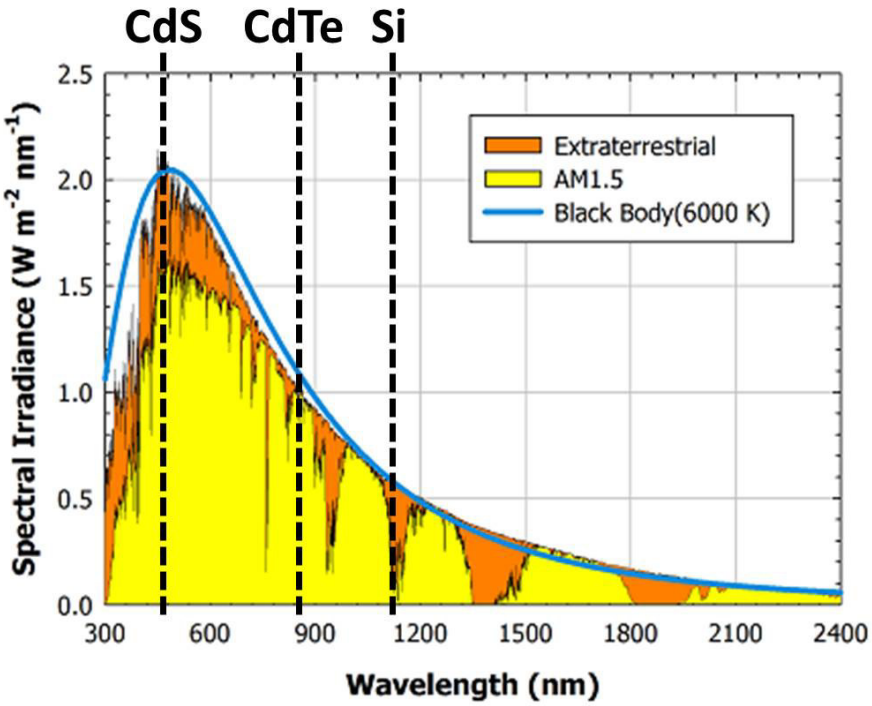

Figure 2.2: the black body spectrum emission is dashed, AM0 is the solar spectrum outside the atmosphere, AM1.5 is the solar spectrum on the earth ground, with a solar zenith angle of 48.2° (standard radiation used to compare solar cells) [6].

Looking at figure 2.2, the graph is cut by dashes indicating the wavelength below which the labelled material absorbs the radiation. In other words, the window layer absorbs the photons with an energy higher than its band bap, while the absorber material absorbs the photons with an energy included between its band gap and the one of the window layer.
Furthermore, the p-type semiconductor should be a direct band gap material, in order to have a very high absorption coefficient. In this way, all the light is absorbed near the junction, where the drift field is present (in the depletion region), which promotes the transition of the minority carriers (electron in this case) through the junction, before they recombine. Silicon is an indirect band gap material, for this reason a thicker layer to absorb all the solar light is needed.
Depositing the material, it is important to obtain crystalline, well oriented and columnar grains; in fact, if grain boundaries cut transversely the material, they prevent the carriers transition.
Regarding the polycrystalline PV of second generation, in comparison with silicon, materials with a band gap more suitable for absorption have been investigated and utilized, as well as more stable materials over time. This has raised the maximum theoretical efficiency achievable.
On the other hand, it is more difficult to obtain high efficiency values, especially at an industrial level, due to the complexity of the processes necessary to have effective heterojunctions.

Moreover, it is important to pay attention to the presence of grain boundaries, since, like defects, they reduce the device efficiency by encouraging the diffusion of impurities. Finally, a downside could be the presence of toxic atoms, such as cadmium [3].

2.1.2 Amorphous thin films

Solar cells can be fabricated also with amorphous thin films: silicon is the most utilized material for this type of cells.
An amorphous material presents a chemical structure similar to a crystalline one, but the lattice is completely disordered. Both in the crystalline and in the amorphous silicon, each atom forms a covalent bond with four other atoms, but to have a disordered lattice the presence of different bonds is needed. In the amorphous silicon used for solar cells, many atoms form three bonds with silicon atoms, and one with a hydrogen atom.
Despite having a non-direct band gap, hydrogenated amorphous silicon presents an absorption coefficient similar to that of a direct band gap semiconductor, for this reason it absorbs all the light near the surface and a thin layer can be used. On the other hand, compared with crystalline silicon, it has weak transport properties as low carrier's mobility and a short lifetime [3].
In conclusion, compared to crystalline, amorphous silicon is cheaper: it allows saving on the amount of material and on the production costs as it needs lower fabrication temperatures, moreover it allows the use of cheaper substrates. On the other hand, the efficiency has also been reduced; the conversion record is 14.0%, and there has been no significant improvement for twenty years, as evidenced in figure 2.1 [4].

2.2 Principles of photovoltaic cells operation

The fulcrum of solar cells operation is the establishment of a p-n junction, that is the connection of a p-type semiconductor with a n-type. At the interface, the respective concentration gradients drive the holes in the n-region, and the electrons in the p-region. Close to the junction, this migration causes the annihilation of the free electrons in the n-type and of the free holes in the p-type semiconductor, forming the so-called depletion region or space charge region (W). In this region the ionized atoms' density abundantly overhangs the free carries density. Considering the "full depletion approximation" of free carriers, the space charge density ρ (x) presents a similar trend to that indicated in fig. 2.3a:

$$\rho = eN_D \text{ for } 0 < x < x_n$$

$$\rho = -eN_A \text{ for } -x_p < x < 0$$

$$\rho = 0 \text{ for } x > x_n \text{ and } x < -x_p$$

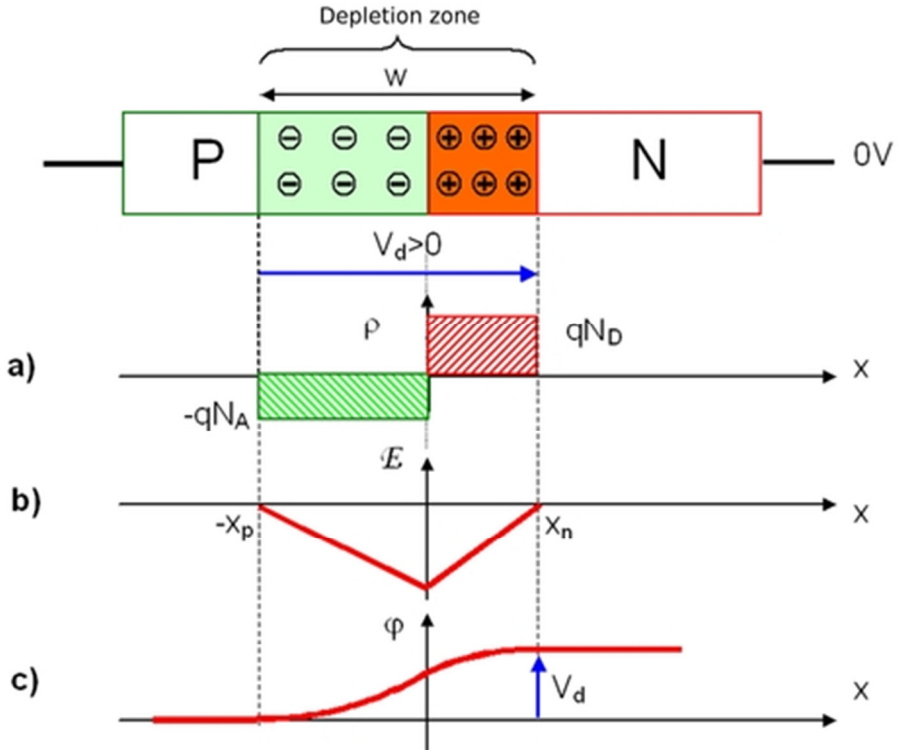

Figure 2.3: the p-n junction and through the depletion region: 2.3a) "step approximation" of the charge density trend, 2.3b) the electric field trend, and 2.3c) the electrostatic potential trend [7].

Where N_A is the net acceptors density in the p-region, N_D is the net donors density in the n-region, and "e" is the elementary charge.
This space charge generates an electric field, called Drift field or Built-in field, directed from the n-type to the p-type region, which pushes the holes to the left, and the electrons to the right. In that way at the equilibrium the drift currents compensate the diffusion currents. This Drift field is also the responsible for the hole-electron separation after the formation of the couple through the photon absorption.
The Drift field E(x) trend is indicated in fig. 2.3b, it is null in the asymptotic neutral regions while its absolute value is maximum at the junction (x = 0).
Finally, in fig. 2.3c the electrostatic potential φ(x) trend is shown, where V_d is the Built-in potential:

$$V_d = \varphi(x_n) - \varphi(-x_p)$$

$$\varphi(x_n) = \varphi(+\infty) \text{ and } \varphi(-x_p) = \varphi(-\infty)$$

As in the asymptotic regions these relations are valid:

$$p(-\infty) = N_A = p_i^{-\frac{e\varphi(-x_p)}{KT}}$$

$$n(+\infty) = N_D = n_i^{-\frac{e\varphi(x_n)}{KT}}$$

where K is the Boltzmann constant, T is the absolute temperature, p is the concentration of free holes and n of free electrons, and $n_i = p_i$ is the concentration of free charges for an intrinsic semiconductor and it is a function of temperature.
And as under thermal equilibrium the equation for the mass action law for semiconductors is:

$$pn = n_i^2$$

Approximating the junction as extended on a single semiconductor, V_d can be expressed according to the characteristics of the junction:

$$V_d = \varphi(x_n) - \varphi(-x_p) = \frac{KT}{e}\log(\frac{N_A N_D}{n_i^2})$$

Formulating the Poisson equation with the appropriate boundaries condition, the electronic potential can be obtained from the charge distribution:

$$\frac{\partial^2 \varphi(x)}{\partial x^2} = -\frac{\rho(x)}{\varepsilon} = -\frac{e}{\varepsilon}(p(x) - n(x) + N_D(x) - N_A(x))$$

Where ε is the permittivity of the semiconductor.
Moreover, considering the condition of global charge neutrality:

$$\int_{-\infty}^{+\infty} \rho(x)dx = 0$$

which, under the "full depletion approximation", it is simplified in:

$$N_A x_p = N_D x_n$$

$$W = x_p + x_n$$

It results that:

$$W = \sqrt{\frac{2\varepsilon}{e}(\frac{1}{N_A} + \frac{1}{N_D})V_d}$$

$$E(0) = -\frac{eN_A x_p}{\varepsilon} = -\frac{eN_D x_n}{\varepsilon}$$

$$V_d = -\frac{E(0)}{2}(x_n + x_p)$$

Moreover, in a semiconductor, the continuity equations for electrons and holes must be satisfied:

$$\frac{\partial n(x,t)}{\partial t} = \frac{1}{e}\frac{\partial J_n}{\partial x} + G_n - R_n$$

$$\frac{\partial p(x,t)}{\partial t} = \frac{1}{e}\frac{\partial J_p}{\partial x} + G_h - R_h$$

Where J_p and J_n are holes and electrons current density respectively, t is the time, G is the generation ratio due to optical or thermal energy and R is the recombination ratio including radiative (photon emission) and non-radiative (phonon emission) mechanisms.
Under illumination the main generation process is the photo-generation, which is the creation of electron-hole pairs through photons absorption. Near the junction, the Drift field separates the electrons from the respective holes, driving them into opposite directions, creating a current: this is the photovoltaic effect.

Therefore, from an electronic point of view (see figure 2.4), it is possible to describe a solar cell as a current generator in parallel to a diode (substantially diodes are p-n junctions). To obtain a more realistic description, the model must be integrated at least with a series (R_s) and a parallel (R_p or R_{sh}) resistance to the diode. The series resistance represents the resistivity of the materials and the not perfect ohmicity of contacts, while the parallel resistance represents the defects in the semiconductors such as grain boundaries or spurious phases with low resistance through which the carriers could pass.

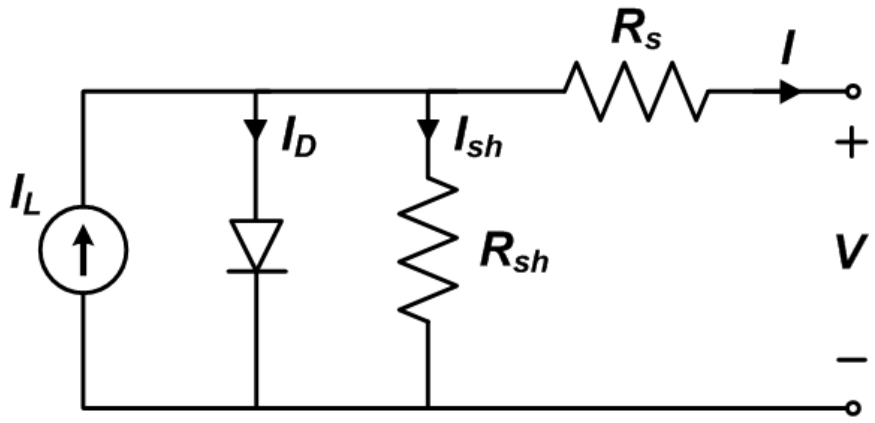

Figure 2.4: equivalent circuit of a solar cell [8].

This circuit could be described by the following relation:

$$J(V) = J_0(e^{\frac{e(V-JRs)}{NKT}} - 1) - J_L + \frac{V - JR_S}{R_P}$$

Where J is the current density, J_0 is the reverse saturation current of the diode, V is the potential difference between the ends of the load resistance R_C, N is the ideality factor. The first item represents the current flowing through the diode, J_L is the generated photocurrent, $\frac{V - JR_S}{R_P}$ represents the current that passes through the parallel resistance and JR_S is the voltage drop on the series resistance.
During light operation, when the external contacts are shunted, J_L flows and it is usually called Short Circuit Current (J_{SC}), on the other hand when no load is connected to the contacts, a voltage called Open Circuit Voltage (V_{OC}) is present between back and front contacts.
The above described model shows that the presence of series and parallel resistances in the cell implies a decrease respectively of the J_{SC} and of V_{OC}, therefore an overall decrease in cells efficiency (as it will be explained in chapter 5).
This is the reason why it is so important to use low resistance materials, to form ohmic contacts with low resistance, to avoid spurious phases, to passivate the grain boundaries, which also favor the carrier's recombination.

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3
CdTe solar cells

With their respective efficiency record of 22.1 % [1] and 22.9 %, CdTe and CIGS thin film solar cells have both reached efficiencies near 26.7 % of crystalline silicon technology [2]. Although CIGS devices are slightly favored in terms of efficiency, CdTe solar cells are the second most common PV technology in the world marketplace after crystalline silicon, currently representing 2.3% of the world market [3]. This is because CdTe is a stable binary compound that evaporates congruently, so that it can be easily deposited in a wide variety of methods; for this reason scaling the laboratory process on large industrial scale is much less complicated than for CIGS.
Usually CdTe based solar cells consist of four parts: the front contact (negative pole), the window layer, which is the n-type of the junction, the absorber CdTe, which is the p-type of the junction, and the back contact (positive pole). All these parts are deposited on a supporting substrate.
Two different device configurations are possible: substrate or superstrate. On the left of figure 3.1 substrate configuration (or front wall) is presented. On the substrate the positive contact, the CdTe, the window layer and the negative contact are deposited in order. The light passes through the window layer and the negative contact, so they must be transparent, while the substrate may not be.
As schematized on the right of figure 3.1, in superstrate configuration (or back wall), the negative contact, the window layer, the CdTe and the front contact are deposited in order on the substrate. Again, the window layer and the negative contact must let the light pass, but in this case the substrate must be transparent too.
To date, CdTe based solar cells with highest efficiencies have been obtained in superstrate configuration, using soda lime glass (SLG) as transparent substrate [4].

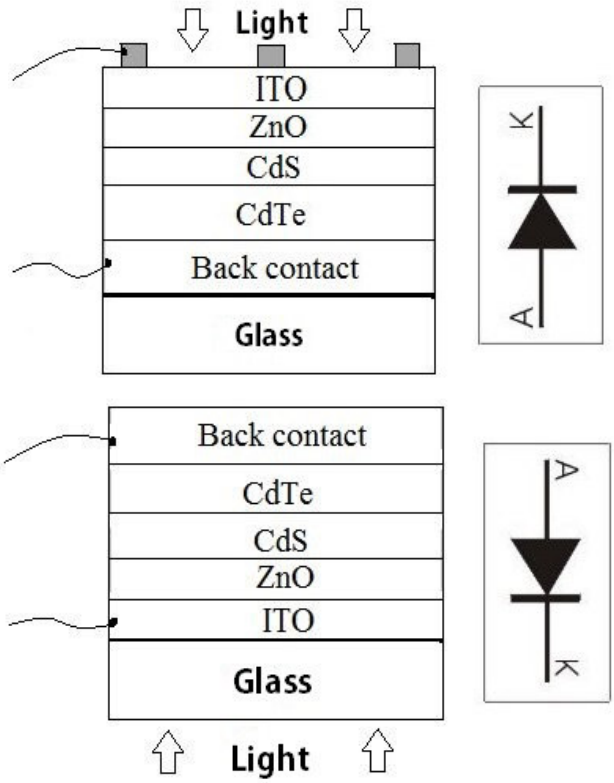

Figure 3.1: the possible device configurations: substrate (left) and superstrate (right).

3.1 The absorber layer: CdTe

CdTe is one of the most important thin film photovoltaic materials. It is a semiconductor with an ideal band gap for solar energy conversion: around 1.5 eV for single crystal [5] and 1.45 eV for polycrystalline form [6]. In principle CdTe could deliver around 1 V [5] of open circuit voltage and 30 mA/cm^2 of short circuit current, for this reason a theoretical maximum efficiency over 30% is achievable [7]. Operatively an efficiency of 22,1 % has been reached in First Solar laboratory [1]. Moreover, its band gap is direct, and its absorption coefficient is around 10^4-10^5cm^{-1}, implying that just few microns of material are enough to absorb all the light; this is the reason why it could be used in form of thin film [4,8].
CdTe is the layer where the electron hole pair generated is separated by the drift field, producing the photovoltaic effect, for this reason it is called absorber layer.
It can be doped both p-type with copper, silver or other I or V group elements, or n-type with boron, aluminum, indium or gallium. On the other hand, being polycrystalline, there is the risk that these metals segregate in the grain boundaries, giving origin to highly conductive metal lines that shunt the p-n junction. Generally, it is self-doped by native defects: it is p-type when there is Cd-vacancy (or Te-excess), or n-type when there is Te-vacancy (or Cd-excess).
Another favorable point is that it is the only stable compound of the Cd-Te phase diagram, and it sublimates congruently. After the deposition an "activation treatment", that is an annealing in presence of chlorine, is necessary (see section 3.2).

Very often CdTe market is hampered by the toxicity of Cadmium, but the fact that cadmium telluride is a stable, insoluble in water and non-volatile compound must be considered. In fact, CdTe is not reputed to be a highly dangerous material such as pure cadmium, and it is not classified as a carcinogen; it can be touched without risks of having cadmium release [9]. The problem could arise if the CdTe decomposed; in the atmosphere this happens with temperatures exceeding 1000 degrees Celsius. Heating a CdTe module to temperatures up to 1100 °C, in order to simulate the exposure to residential and commercial building fires, Fthenakis, et al. [10] showed that 99,96% of the Cd remained encapsulated in the molten glass matrix.
The operation of CdTe panels does not generate any Cd emissions, while, coal burning, steel production, fertilizer production/use, and zinc coatings routinely generate Cd during operation [11].

3.2 The activation treatment

As already mentioned in section 3.1, after CdTe deposition an "activation treatment", that is an annealing in presence of chlorine, is necessary to recrystallize the layer enhancing the grains size and to remove the structural defects. This step is fundamental to reach high efficiencies, otherwise they do not exceed 5 %.
In the case of Cadmium Sulfide (CdS) as window layer, the activation treatment favors the formation of an intermixed layer at the interface, which reduces the lattice mismatch. The two materials tend to mix according to their phase diagram, producing a ternary compound CdS_xTe_{1-x} and a graded bandgap structure in place of an abrupt-interface; in this way the number of interface states due to the different lattice parameter is minimized [12,13]. This intermixed layer allows the hetero-junction to behave as a homo-junction.
The activation treatment can be done annealing the CdTe/CdS stack in a mixture of Ar and a gas containing chlorine, usually difluorocloromethane (HCF_2Cl named Freon).
Otherwise, it can be done by depositing $CdCl_2$ on top of CdTe by evaporation or by wet deposition (in this case using a $CdCl_2$–methanol solution), and subsequently annealing the stack. In both cases an annealing around 400°C is needed [14]. This latter method is the most utilized, especially in the industrial production. $CdCl_2$, however, is a highly toxic and carcinogenic chemical agent, for this reason its usage and disposal need strong safety procedure. Lots of studies have been performed looking for a suitable $CdCl_2$ substitute; recently $MgCl_2$ has been successfully employed [15]. The topic will be further explored in chapter 7.

3.3 The window layer

The window layer has to be a n-type semiconductor, which coupled with CdTe forms the p-n junction.
Up to now, cadmium sulfide has been the most used window layer in CdTe based solar cells, but also in CIGS devices. The reason is its high band gap of 2.42 eV, which allows the visible part of the solar spectrum to reach the absorber. The role of the window layer is favored by minimizing the thickness, because the light passing through the layer is absorbed according to the Bouguer law:

$$I = I_0 e^{-\alpha t}$$

Where α is the absorption coefficient, t is the thickness of the layer, and I_0 and I are the intensity of the incident light and the intensity of the light passed through the thickness t of the material, respectively. Thus, as the absorption coefficient and the thickness of the material increase, the amount of light absorbed in the n-type semiconductor increases.
On the other hand, a very thin layer enhances the defects incidence: the thickness may not be uniform and in the worst case the presence of pin-holes is possible, which, connecting directly the CdTe to the negative contact, could shunt the device. Moreover, CdS is one of the active material in the device, because the photovoltaic effect depends on its presence, thus, a thicker layer than the depletion region thickness is needed [8].
CdS has the advantage of forming the CdS_xTe_{1-x} intermixed layer with CdTe instead of an abrupt-junction, reducing the reticular mismatch and thus the presence of interface states. On the other hand, also a thin layer of CdS absorbs some of the light spectrum, due to its band gap. For this reason, to increase the cell short circuit current and exceed 20% efficiency, alternative window layers with higher band gaps have been experimented. Currently, the one that is having more success is the Magnesium Zinc Oxide (MZO) [16,17]. The topic will be further explored in chapter 6.

3.4 The front contact

The front contact must be a transparent and highly conductive material, for this reason TCOs (Transparent Conductive Oxides) are used. These oxides show a transparency of about 90% of visible light and a high n-type conductivity. Generally, the wide energy gap materials are electric insulators and they are characterized by good transparency in the visible [18].
To possess transparency and conductivity at the same time, a wide band gap oxide is doped to obtain a degenerate semiconductor. For example, a donor element is introduced into the oxide structure, in this way the concentration of electrons is increased, and therefore the n-type conductivity. Otherwise, the deviation from the correct stoichiometry, such as the presence of oxygen vacancies defects, is exploited. On the contrary, the substitution of a low valence cation with an acceptor impurity creates a hole that behaves as a trap in the oxide, decreasing its n-type conductivity [8].
TCOs used for photovoltaic applications must be physically and chemically stable, because they do not have to degrade over time nor release impurities that could diffuse into the devices; this is especially true in superstrate configuration, as they must resist to the deposition process of all the layers.
The most utilized are: tin doped indium oxide (In_2O_3:Sn or ITO), fluorine doped tin oxide (SnO_2:F or FTO), aluminum doped zinc oxide (ZnO:Al or AZO) and cadmium stannate (Cd_2SnO_4). Above this conductive layer a thin layer (from 50 to 200 nm) of a buffer material is usually deposited, such as tin oxide (TO), zinc oxide (ZnO) or gallium oxide (Ga_2O_3). The buffer has the task of avoiding the diffusion of sodium and potassium atoms from glass or metal atoms from TCO. Moreover, with a very thin window layer, where pin-holes presence is possible, the buffer layer prevents the cell from short circuits [8].

3.5 The back contact

The back contact is deposited on top of the absorber and does not face the light. Since CdTe has a very high electron affinity and requires a back contact with a work function higher than 5.7 eV, finding a material to make a good ohmic contact is hard [8]. Generally, it is fabricated with compounds containing copper. It is thought that copper is necessary, because it diffuses in CdTe increasing the carrier concentration, thus forming a p^+ region near the back contact which allows the carrier to go through the barrier. Anyhow, even just considering the obtained devices, the insertion of copper has demonstrated to bring the highest efficiency. On the other hand, the diffusion of copper into CdTe over time seems to be the main cause of degradation of these solar cells. Before copper deposition, usually, a chemical etching of the CdTe surface with Bromine-Methanol (Br-MeOH) or Nitric-Phosphoric acid (HNO_3/HPO_3) is performed [8]. In case of chlorine treatment in air, this etching removes the surface oxidation, but in any case it enriches the surface of CdTe in tellurium, making it more p-type, thus favoring the ohmicity of the contact. Moreover, the tellurium enrichment favors the formation of a thin Cu_2Te layer, or others Cu-Te compounds, which limit the copper diffusion into the CdTe [19,20].
The copper diffusion into CdTe bulk through the grain boundaries could shunt the device; for this reason it has always been thought that copper should be avoided to have stable devices for 20-30 years [8]. Recently, MoO_x has been applied as back contact to high temperature deposited CdTe (by close space sublimation), performing good efficiency [21]. On the other hand, applying it to low temperature devices does not seem that easy. This topic will be further explored in chapter 8.1.
Other more incisive solutions are being studied, as the use of a minimum amount of copper, or an innovative wet Cu deposition method. They will be deepened in chapters 8.2 and 8.3.

3.6 The substrate

A substrate must have appropriate characteristics to be utilized in thin film solar cells: low roughness, mechanical and thermal resistance and good adhesion with the first layer of the deposition sequence. Moreover, for large photovoltaic panels (the standard size is 120 x 60 cm^2), the substrate must be cheap to avoid affecting the cost of the final device; for this reason the common glass (soda lime glass) is the most used.
Otherwise, alkali-free glass can be used. It ensures that no polluting species (such as sodium) are released into the film and it allows more freedom in the choice of growth processes, being resistant to higher temperatures.
Moreover, the market is looking for new materials that, in addition to the above listed features, can better adapt to the shape of buildings, and can make the cells lighter and more flexible. For example, for substrate configuration cells, where transparency is not necessary, polymeric substrates are being studied [8]. But also in superstrate configuration, using a low temperature process, high efficiencies have been reached on flexible transparent substrate such as polyimide films and ultra-thin glasses [22].

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4
Deposition of thin films

4.1 Sputtering deposition method

Sputtering is a widely used deposition method. It is part of the physical vapor deposition techniques: practically, it is one of those methods in which physical mechanics or thermodynamics are exploited to deposit.
Substantially, through ion bombardment a large amount of energy is supplied to the material that has to be deposited (source or target), and because of the high energy acquired, the bonds between the atoms are broken, thus they are free to leave the surface of the source [1].

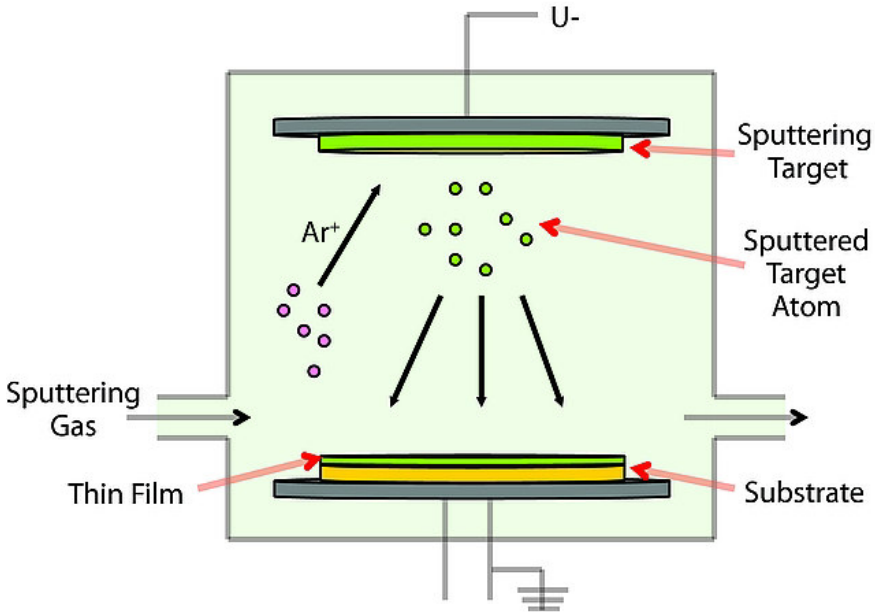

Figure 4.1: example of sputtering working principle scheme [2].

The sputtering machine consists of a vacuum chamber, where two plates are arranged face-to-face, at 5-10 cm of distance (see fig. 4.1, where a sputtering system with vertical architecture is presented). One is made of the material to be deposited (target), while the other one is holding the substrate. Once achieved ultra-high vacuum (10^{-6}-10^{-7} mbar) in the chamber, a gas is introduced, generally a noble gas (such as Argon), up to a pressure of 10^{-4} - 10^{-2} mbar. A potential difference is applied between the plates; the target is negatively polarized (cathode), while the substrate holder acts as a positive pole (anode). By increasing the potential applied, the free electrons inside the chamber (generated by cosmic rays) are accelerated to sufficient energies to ionize the gas, thus a glow discharge occurs. The gas ions are accelerated towards the cathode, they bombard the material and they extract atoms that are deposited on the substrate. With this technique the particles reach the substrate with a higher energy than in evaporation processes: typically, the "sputtered" atoms arrive on the

substrate with energies around 1-10 eV, while the energies related to thermal techniques (evaporation) are around 0.1 - 0.5 eV. This imply a higher surface mobility, which favors the minimization of free energy, thus an ordered arrangement of atoms and a better crystallization.
Another effect of the Ar^+ ions bombardment is the emission of electrons from the target (secondary electrons), which are accelerated, gaining energy and consequently contributing to the noble gas ionization.
The DC (direct current) is the simplest type of sputtering, where the ions are accelerated with a continuous electric field. This technique is basically used for conductive materials while depositing semiconductors is very difficult, and insulators is even impossible. If the materials are not conductive, with DC sputtering they are not able to dispose of the charges accumulated during the bombardment, thus on the surface of these targets a charged coating tends to form, which is able to stop the discharge and the whole process.
To deposit semiconductors and insulators a RF (radio-frequency) sputtering is needed; in this case an alternating potential difference is applied between the plates. At each half-period there is an inversion of the polarization, and the electrons oscillate into the glowing region, acquiring sufficient energy to ionize the gas. If a low frequency alternative potential is applied, at each half-period the substrate is heavily bombed by the ions, and the condensed film is removed (back sputtering), otherwise, using high frequencies, the ions are not able to reach the target [3]. To overcome this problem, the target is coupled to the radiofrequency via a proper capacitor: thus, during the first half period (positive) there is a high electron current at the anode, while in the negative half period there is a small ionic current, because of the lower mobility of the ions that are still near the cathode.
Moreover, considering that the electrodes potentials are reverse proportional to the fourth power of their respective areas:

$$\frac{V_1}{V_2} = \left(\frac{A_2}{A_1}\right)^4$$

to further enhance the cathode negative potential, its surface must be smaller than the substrate area, for this reason the substrate holder is usually connected to the walls of the vacuum chamber.
In this way it is possible to bomb the target, without damaging the growing film [4].
A further variant exists: the sputtering (DC and RF) magnetron, in which behind the target a permanent magnet is set, with the poles arranged in such a way as to produce a magnetic field parallel to the target surface. Therefore, in the region close to the target, under the combined effect of the electric and the magnetic fields (Lorentz force), the secondary electrons are forced on helical trajectories; they stay trapped near the target. This results in a double advantage: the substrate heating decreases and the gas ionization becomes more probable, consequently the sputtering efficiency (the deposition rate) increases up to three times more than in the no-magnetron sputtering. Moreover, to reach equal deposition rates, the gas pressure needed is much lower than in traditional DC or RF systems. This variant, due to the high deposition rate, is the most suitable for industrial applications.

4.2 Vacuum evaporation method

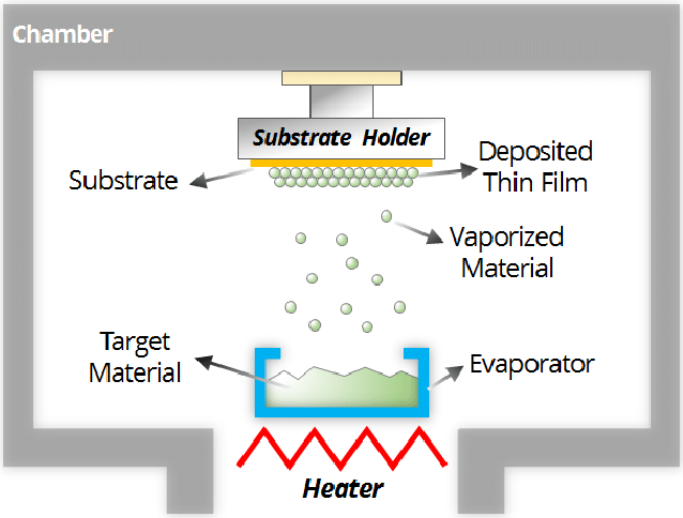

Figure 4.2: vacuum evaporation working principle scheme [5].

Vacuum evaporation is part of the physical vapor deposition (PVD) techniques. It is a process that takes place in a high vacuum chamber. The material to be evaporated is placed in a container (crucible) composed of a metal non-reactive with the material, and which has a high melting temperature (such as tungsten, molybdenum, tantalum). The crucible is suitably shaped, and it is heated up to the evaporation or sublimation temperature of the material contained therein. The evaporation can be from solid or liquid phase. The vaporized material reaches the substrate, which is placed above the crucible, and, if the substrate temperature is lower than the condensation temperature of the evaporating material, it condenses (see the scheme in figure 4.2).
The material adheres to the substrate mainly from a single direction (angle of view of the crucible), thus if the substrate has a rough surface, the protrusions prevent the material from covering some areas, with a shadow effect, resulting in a not uniform film. Therefore, in the most advanced systems, the substrates are rotated to uniformly cover the surface roughness and ensure a greater homogeneity of the film. In any case, the substrate must resist the temperature at which the film is deposited and it must be as smooth and clean as possible.
Heating the substrate improves the crystalline growth of the film: in fact, a hot substrate provides energy to the atoms, increasing their superficial mobility and favoring the minimization of free energy.
Performing this process inside a vacuum chamber is crucial in order to reduce the particle density of undesirable atoms and molecules (contaminants). The higher is the vacuum, the longer is the mean free path of the atoms: for example, at a pressure of 10^{-5} mbar, the mean free path of atoms is about 10 m. In addition, a higher vacuum implies a lower evaporation temperature. Moreover, for some types of materials the risk of incorporating (adsorption) the residual gas in the film is present.
While metals generally evaporate as single atoms and sometimes as groups of atoms (clusters), compounds rarely evaporate as molecules; often they dissociate and the individual

elements evaporate at different rates. Consequently, the composition of the film can differ from that of the starting compound. In the worst cases, one of the components evaporates so faster than the others, that they remain as residual; in this case the components must be evaporated separately (co-evaporation).
Working with oxides, films grow poor in oxygen, therefore a proper partial pressure of oxygen is introduced into the chamber.
Regarding metal alloys, the components evaporate almost independently from each other: if their vapor pressure are too different during the evaporation, the film grows enriched in the component with the higher vapor pressure. To obtain the wanted composition, a starting compound rich in the less volatile component is needed.
The evaporation rate can be tuned changing the temperature of the source. A better crystallization is obtained using low rates (in the order of 1 Å/sec or less); in that condition it is more probable that atoms arrange in an orderly pattern.
Depending on the heating method, different kinds of vacuum evaporation exist. The simplest one consists in a flow of high current through the crucible, which heats the source by Joule effect. Otherwise, a high-power laser can be used to vaporize the material. Moreover, an electron beam emitted by an incandescent tungsten filament and accelerated by a proper potential difference, can be used to evaporate the source; this is called electron gun. Generally, the filament is placed under the crucible and the electrons are driven in a curved trajectory of 270 ° by a magnetic field; this to prevent to damage the filament with evaporated material [6].

4.3 References

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5
Characterization of solar cells

5.1 Current-Voltage (J-V)

The first fundamental characterization is the J-V, that is the study of the current density-voltage graph associated with the device, from which the parameters to calculate the efficiency of light-energy conversion are extracted. Ideally, the J-V characteristics are measured with the spectrum of the sun with an illumination density of 100 mW/cm^2, which is the standard value universally used to determine the efficiency of a photovoltaic cell, also called AM 1.5 standard radiation (corresponding at a solar zenith angle of 48.19 °, at a temperature of 25 ° C), also considered as "1 sun". For this reason, a solar simulator is needed, or at least a lamp that can reproduce this spectrum.
Practically, the cells are tested by fixing the value of the incident power, the temperature (which is the room temperature 20-25 ° C) and the surface area.
The cell is exposed to radiation and the contacts are connected to a voltage-current generator. A voltage ramp is supplied to the cell and at the same time the current flowing through the device is measured; in this way a voltage-current (or current density) graph is plotted (see figure 5.1).

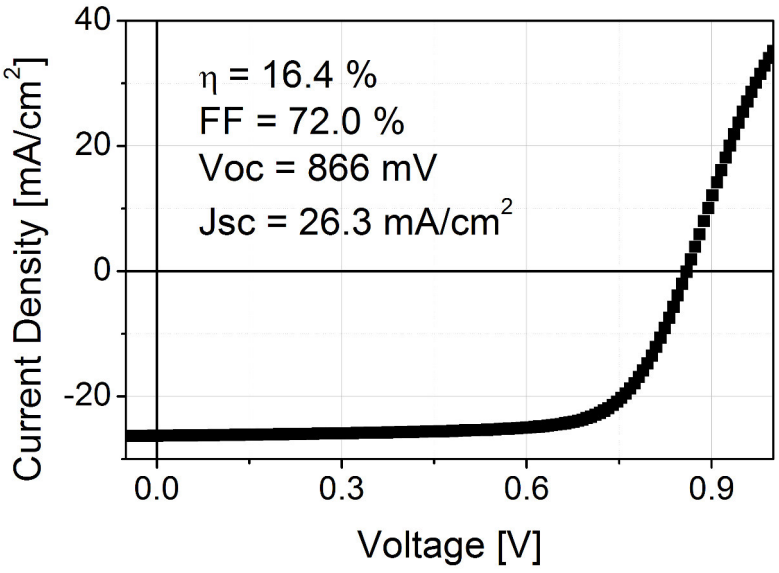

Figure 5.1: current density – voltage plot of a solar cell fabricated in LAPS

A diode characteristic translated into the fourth quadrant by the action of the photovoltaic effect is obtained. Substantially, the photovoltaic device is a large diode that provides electric power when illuminated.

When the voltage supplied by the external generator is null, and in the cell the separation process of the electron-hole pairs occurs due to the incident radiation, a negative current value is measured: this value is the short circuit current of the cell (I_{SC}) or short circuit current density (Jsc) if I_{SC} is divided by the area.
Then the external generator starts to supply an increasing voltage, which is opposed to the potential difference (d.d.p.) between the ends of the depletion region. When the two d.d.p. have the same value, the current is deleted: the value of the voltage read at this point is the open circuit voltage of the cell (V_{OC}). Further increasing the applied tension, the current takes positive values because the voltage supplied by the generator is greater than the drift field V_d, and therefore electrons flow towards the positive contact (and holes towards the negative contact).
The conversion efficiency of a cell is measured in terms of ratio between the maximum power that can be delivered by the cell and the power of the incident radiation:

$$\eta = \frac{P_{\max}}{P_{in}}$$

The optimal working condition of the cell is represented by the point of the J-V characteristic corresponding to the maximum product voltage-current, which expresses the electric power obtainable:

$$P_{\max} = I_{\max} V_{\max}$$

Moreover, a fill factor (FF) is defined as:

$$FF = \frac{I_{\max} V_{\max}}{I_{SC} V_{OC}}$$

This parameter indicates the ratio between the maximum real extractable power and the maximum ideal obtainable power, in practice it indicates how much the cell approaches its ideality.
From this, efficiency is formally defined:

$$\eta = \frac{I_{SC} V_{OC} FF}{P_{in}} = \frac{I_{\max} V_{\max}}{P_{in}} = \frac{P_{\max}}{P_{in}}$$

These key parameters V_{OC}, I_{SC}, FF and η allow to evaluate the performance of the manufactured photovoltaic device and to make a comparison with other cells of whatever laboratory.

5.2 Capacitance-Voltage (C-V)

Capacitance-Voltage is a characterization used to study the structure and properties of the semiconductors; it can estimate the net fixed charge density Na-Nd, which is the difference between the acceptors and the donors concentration. It assumes that a solar cell can be seen as a capacitor, where the depletion region acts as an insulator and the neutral regions as conductors.
Moreover, the "full depletion approximation" is assumed: which considers the depletion region empty of free charges and spatially defined, i.e. an abrupt transition between the space charge and the depletion region.
Capacitance is defined [1]:

$$C = \frac{Q}{V} = \frac{\varepsilon_r \varepsilon_0 A}{W}$$

Where Q is the electric charge at the ends of the depletion region, V is the voltage, A is the surface, W is the width of the depletion region, ε_0 is the vacuum permittivity and ε_r is the relative permittivity of the material.
The capacitor extends over the CdTe/CdS junction, so the capacitance is:

$$C = \frac{A\varepsilon_0}{\frac{X_n}{\varepsilon_n} + \frac{X_p}{\varepsilon_p}}$$

Practically, it is given by two series connected capacitors, one extended in the depletion region in the CdS (X_n) and one in the CdTe (X_p).
It is also possible to write:

$$C = \sqrt{\frac{qX_n X_p N_A N_D}{2\left(N_A X_p + N_D X_n\right)\left(V_{bi} \pm V_{DC}\right)}}$$

Where N_A and N_D are the acceptors and donors concentration respectively.
Therefore, the capacitance at the ends of the cell has to be measured as a function of the applied voltage; if an alternating signal (V_{AC}) is overlapped to the DC signal, the system response can be expressed as a development of function in series:

$$C = C_0 + C_1 \partial V_{AC} + C_2 \left(\partial V_{AC}\right)^2 + \ldots$$

The alternating signal is essential for the measurement, as the instruments extrapolate the value of the capacitance from the reactive component of the alternating current that circulates in the device due to the applied alternating voltage; if the applied tension was only direct, the current would be null. In any case, if the alternating signal has a sufficiently small amplitude, it is possible to consider the system linear and take into account only the dependence from the V_{DC}.

Regarding CdTe/CdS solar cells, since the n-type semiconductor (CdS) is much more doped than the p-type (CdTe), the depletion region can be considered almost completely extended in CdTe. Consequently, considering the density (N_A) of a single acceptor state near the valence band, the width of the depletion region can be written:

$$W = \sqrt{\frac{2\varepsilon_p \varepsilon_0 (V_{bi} - V_{DC})}{qN_A}}$$

Then:

$$C = \frac{\varepsilon_p \varepsilon_0 A}{\sqrt{\frac{2\varepsilon_p \varepsilon_0 (V_{bi} - V_{DC})}{qN_A}}}$$

Therefore, by applying a voltage ramp to the cell, and measuring the capacitance, the graph is obtained (see figure 5.2).

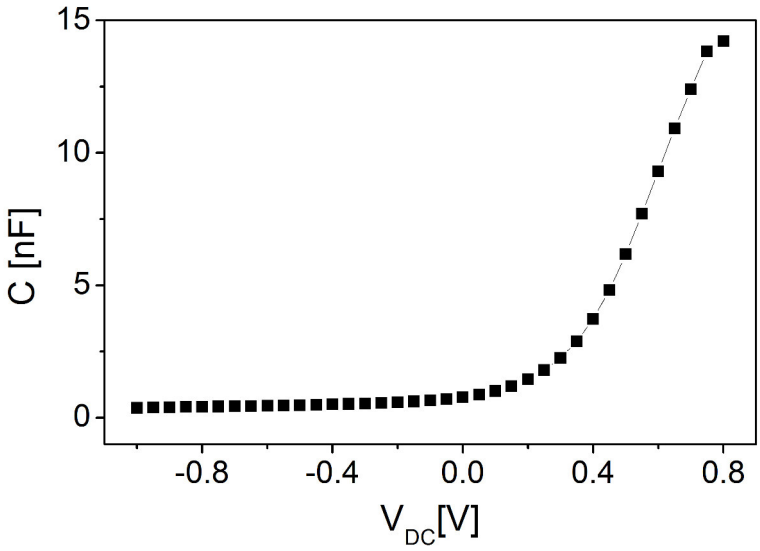

Figure 5.2: C-V curve

Subsequently the Mott-Schottky equation (and curve, see figure 5.3) can be obtained [2]:

$$\left(\frac{A}{C}\right)^2 = \frac{2(V_{bi} - V_{DC})}{\varepsilon_p \varepsilon_0 q N_A}$$

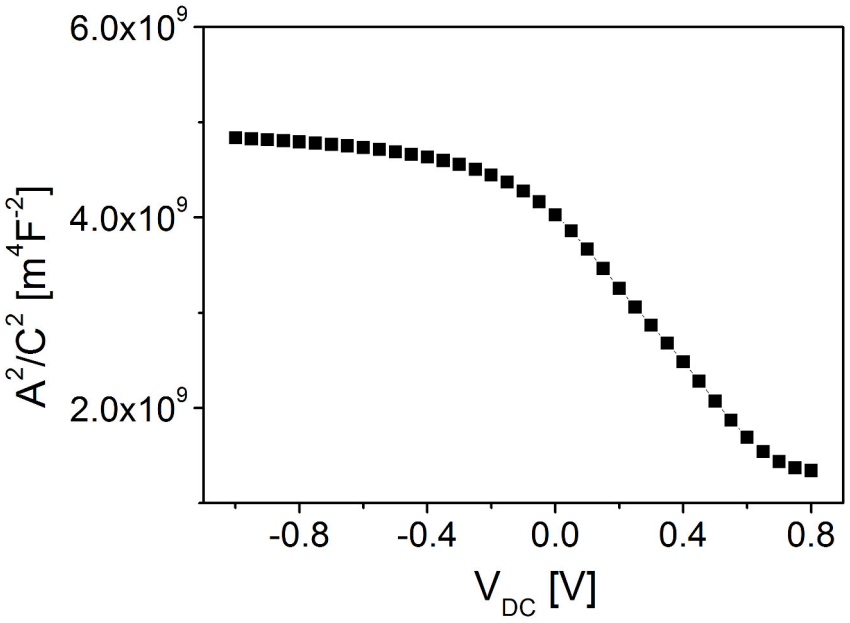

Figure 5.3: Mott-Schottky curve

Because the slope of the curve is:

$$m = -\frac{2}{\varepsilon_p \varepsilon_0 q N_A}$$

Deriving the curve N_A can be extracted for each V_{DC}:

$$N_A = -\frac{2}{m \varepsilon_p \varepsilon_0 q}$$

After N_A extraction, from the intercept p_0 of the Mott-Schottky curve, also the Built-in voltage can be calculated:

$$V_{bi} = \frac{p_0 q \varepsilon_p \varepsilon_0 N_A}{2}$$

At this point, also the width of the depletion region W is quantified.
Consequently, at each N_A value a position within the absorber is assigned; this outlines the doping profile near the junction (see figure 5.4). To clarify, the charging/un-charging cycle given by V_{AC} takes place at the edge of the depletion region, V_{DC} varies the width of the depletion region (selecting a position) and the application of a small V_{AC} allows to probe N_A at that position.

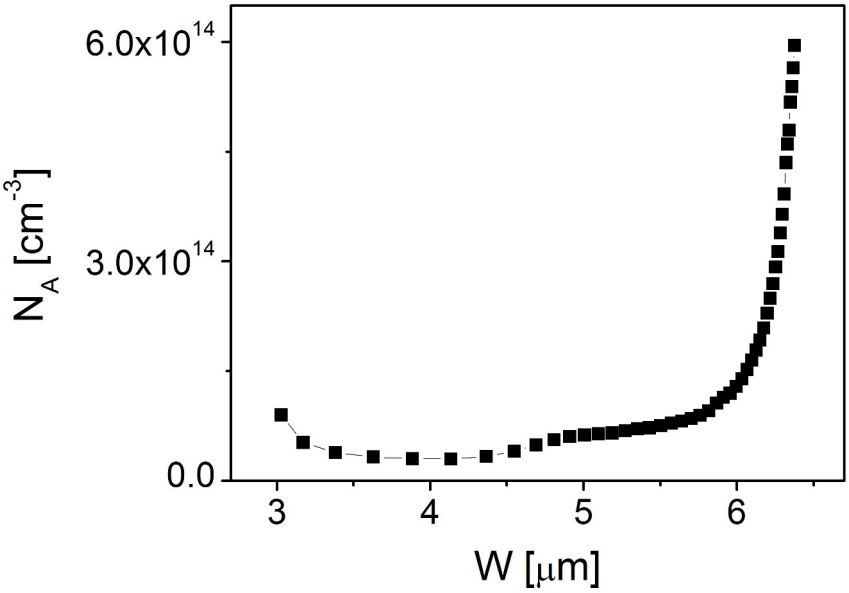

Figure 5.4: doping profile near the junction

At high voltages, the N_A profile assumes an asymptotic behavior, which indicates that the depletion region has reached the maximum extension limit, practically it occupies the whole CdTe layer.
Moreover, at high voltages (V_{DC} > ~ 0.8 V in the case represented in figure 5.5), the presence of the series capacitance of the Shottky diode given by the junction between the metal layer and the CdTe is visible. In fact, while this capacitance is negligible at low DC voltages, as the field increases, it becomes comparable with that of the junction, consequently it reduces the total capacitance value (as shown in figure 5.5). This effect can give an idea of the back contact ohmicity [3].

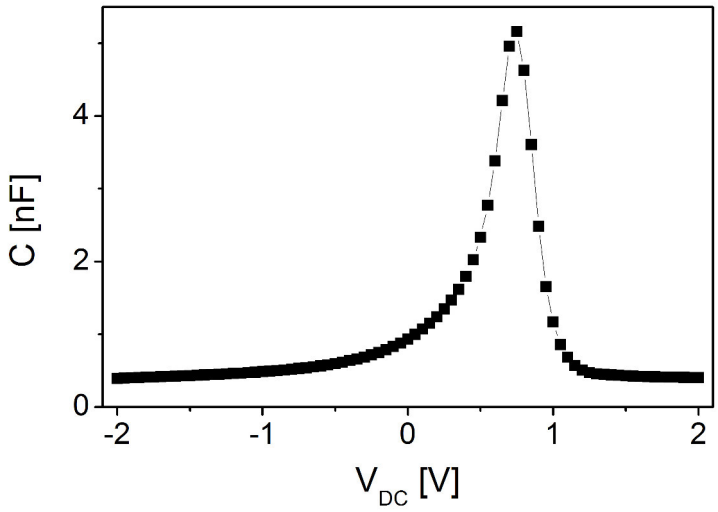

Figure 5.5: effect of the back contact in the C-V graph

So from this study the net fixed charge density (and so also the free carriers density) in the CdTe layer is estimated. In particular, it is determined from the lower part of the U-shape profile, in order to avoid effects due to others factors, such as a not perfectly ohmic back contact and the limited thickness of CdTe [4]. Indeed, this value is only reliable if the defects concentration in the semiconductor is low, because in the above listed calculations N_A is considered as a constant, while actually it varies with the applied voltage.
The accuracy of the results can be verify comparing measurements acquired at different alternating voltage frequencies (usually from 10 kHz to 1 MHz). In fact, different defects respond to electric signals at different speeds, because each defect has its own emission and capture rate. For this reason some can follow high frequency signals and they are defined "fast defects", while others can not thus they are "slow defects". At high frequencies the "slow defects" are frozen out and this reduces the effective number of carriers (as shown in figure 5.6). The bigger is the difference between the N_A-W curves obtained at various frequencies, the larger is the number of different defects.

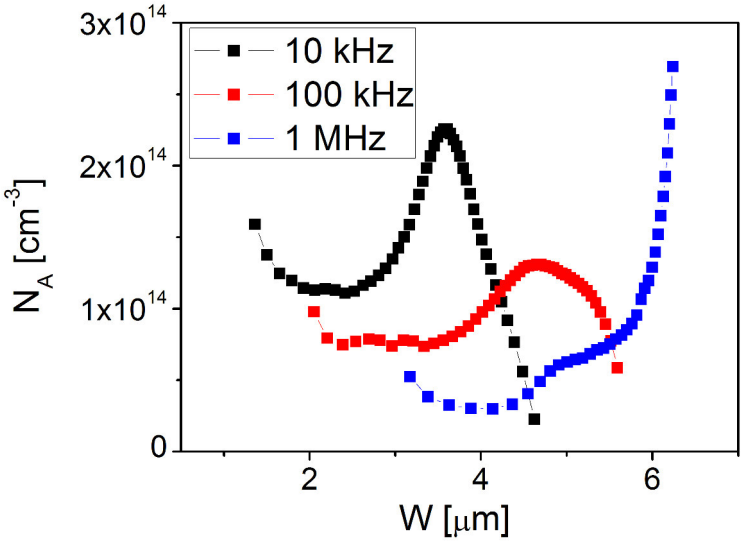

Figure 5.6: defects highlighted by the frequency of the measurement: the black curve is the profile obtained at 10 kHz, the red at 100 kHz and the blue at 1 MHz.

5.3 Drive Level Capacitance Profiling (DLCP)

As explained in the subchapter 5.2, the C-V shows the free charges density profile in the approximation that N_A is the density of a single acceptor state near the valence band [5]. This approximation is valid only if no deep defects are present in the band-gap, because otherwise they contribute to the capacitance, leading to an overestimate of the free charge density and to an underestimate of the length of the depletion region [5,6]. Comparing CV and DLCP profiles the density of deep defects in the depletion region can be estimated. As for CV measurements, when the alternating signal V_{AC} overlaps the DC signal, the response of the system can be expressed as a development of function in series:

$$C = C_0 + C_1 \partial V_{AC} + C_2 (\partial V_{AC})^2 + ...$$

Unlike the CV, in this technique the terms of development further the first are also considered; in fact it is possible to extract useful information also from them. Practically from the relation between the capacitance and the applied AC level (drive level) it is possible to extract the density profile of a specific defect at a specific energy along the depletion region.
The set angular frequency ω and temperature T of the measurement determine the limit energy E_e of the electronic states at which the occupation of a state can change fast enough to follow the alternating signal:

$$E_e = -KT \ln\left(\frac{\omega}{2\pi\nu_0 T^2}\right)$$

Where

$$\nu = \nu_0 T^2 = N_V(T) < v > \sigma_h$$

is the thermal emission prefactor, which depends on the effective density of states in the valence band N_V, on the average thermal velocity <v> and on the capture cross section σ_h of the gap state involved.

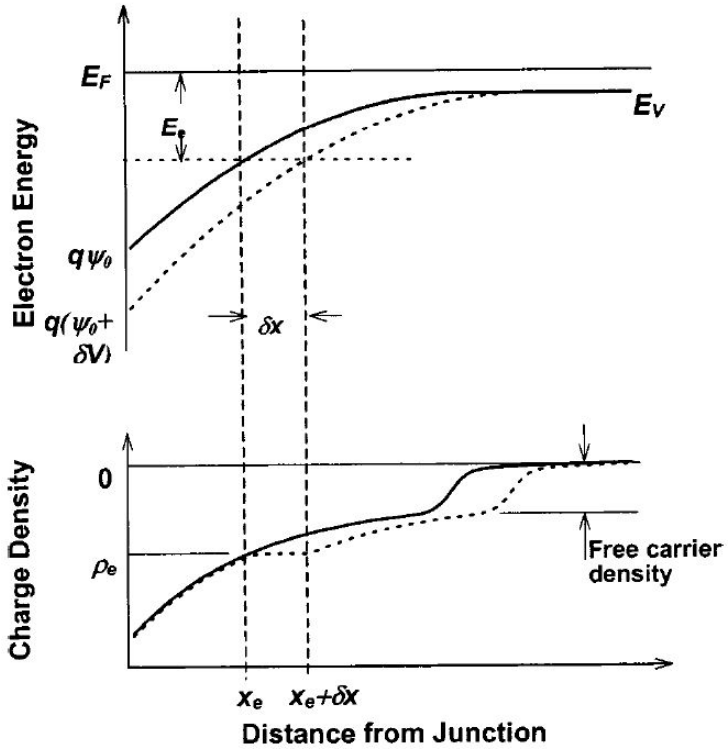

Figure 5.7: the upper part shows the change in band bending when a small bias dV is applied: the solid line and dashed lines indicate the band bending before and after the application of dV, respectively. The lower part represents the corresponding charge densities [5]

Since only the states that differ from the valence band of an energy lower than E_e (in p-type semiconductors such as CdTe) can follow the alternating signal, only these states affect the measurement of the capacitance. x_e is the point in which E_F-E_V=E_e, which is determined by the band bending in the depletion region. Between the interface and x_e the states have not sufficient time to change their occupation, because in this region E_F-E_V>E_e. At longer distance than x_e the states follow the alternating signal and thus they influence the measurement. x=0 means the interface because in CdTe/CdS devices the depletion region is considered as completely extended in CdTe.
Practically two overlapping signals are applied to the cell, one DC and one AC with fixed frequency. The DC voltage bends the bands and the Fermi level, especially near the junction, and at the same time changes the length of the depletion region. The AC voltage has the same effect, but at a certain frequency; it causes the bands to oscillate around the position dictated by the DC voltage.
In general, the DC potential at the interface can be expressed as:

$$\Psi_0(0) = \int_0^{\infty} x \frac{\rho_0(x)}{\varepsilon_p \varepsilon_0} dx = \int_0^{x_e} x \frac{\rho_0(x)}{\varepsilon_p \varepsilon_0} dx + \int_{x_e}^{\infty} x \frac{\rho_0(x)}{\varepsilon_p \varepsilon_0} dx \qquad (1)$$

Where x is the distance from the interface, $\rho_0(x)$ is the charge density without applied AC voltage, ε_p is the relative permittivity of the CdTe, and ε_0 is the vacuum permittivity. Now

adding an alternating potential V_{AC}, the voltage at the interface becomes $\Psi(0) = \Psi_0(0) + \delta V$, and the point in which E_F-E_V=E_e moves farther from the interface in $x_e + \delta x$ (see figure 5.7). So, if δV is applied for a time of order of $\frac{1}{\omega}$, also the states between x_e and $x_e + \delta x$ are not able to follow the signal; practically with the application of the V_{AC} field the response of the defects between x_e and $x_e + \delta x$ is limited. Thus, the charge density at $x_e + \delta x$ is equal to the one at x_e prior to the application of δV, and we called this value ρ_e. Thus, at a time $\frac{1}{\omega}$ following the application of δV the voltage at the interface becomes:

$$\Psi(0) = \int_0^{x_e} x\frac{\rho_0(x)}{\varepsilon_p\varepsilon_0}dx + \int_{x_e}^{x_e+\delta x} x\frac{\rho_e}{\varepsilon_p\varepsilon_0}dx + \int_{x_e+\delta x}^{\infty} x\frac{\rho(x)}{\varepsilon_p\varepsilon_0}dx \qquad (2)$$

Beyond x_e the properties of the semiconductor are roughly constant on a scale of the length of δx, and $\rho(x) \approx \rho_0(x-\delta x)$, thus the final integral in equation (1) will be equal to the final of equation (2).
Thus the total charge variation δQ in the depletion region due to δV is simply the charge between x_e and $x_e + \delta x$:

$$\delta Q = A\rho_e\delta x$$

Therefore the capacitance due to the oscillating field, that with frequency ω alternates the potential at the junction between ψ_0 and $\psi_0 + \delta V$, is:

$$C = \frac{\delta Q}{\delta V}$$

Now expressing δx in terms of δV, and considering $\rho(x) \approx \rho_0(x-\delta x)$ and ρ_e as a constant:

$$C = \frac{A\rho_e\varepsilon_p\varepsilon_0}{\varepsilon_p\varepsilon_0 F_e - \rho_e x_e} - \frac{A\rho_e{}^2\varepsilon_p{}^2\varepsilon_0{}^2}{2\left(\varepsilon_p\varepsilon_0 F_e - \rho_e x_e\right)^3}\delta V + \ldots$$

Where F_e is the electric field in x_e: $F_e = \left|\frac{d\Psi}{dx}\right|_e$,

$$\text{and so } C_0 = \frac{A\rho_e\varepsilon_p\varepsilon_0}{\varepsilon_p\varepsilon_0 F_e + \rho_e x_e}$$

$$\text{and } C_1 = -\frac{A\rho_e{}^2\varepsilon_p{}^2\varepsilon_0{}^2}{2\left(\varepsilon_p\varepsilon_0 F_e + \rho_e x_e\right)^3}$$

The value of C_0 is the same obtained from the CV measurement.
At this point, using C_0 and C_1 it is possible to calculate the ionized gap state density at the distance x_e from the junction:

$$N_{DL} = \frac{\rho_e}{q} = -\frac{C_0^{\,3}}{2q\varepsilon_p\varepsilon_0 A^2 C_1}$$

and the corresponding distance x_e from the junction:

$$x_e = \frac{\varepsilon_p\varepsilon_0 A}{C_0}$$

Since C_0 is the capacitance value when V_{AC} is null, this value of x_e is identical to that obtained from an ideal CV measurement.

Practically, at set temperature and frequency of V_{AC}, V_{AC} voltages with increasing amplitude overlap each V_{DC} voltage.

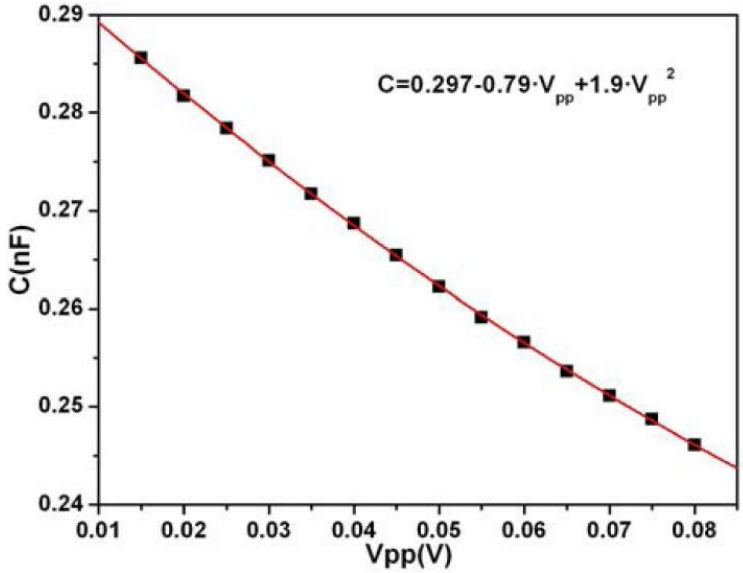

Figure 5.8: C-V_{AC} curve.

Fitting the C - V_{AC} curve (figure 5.8), C_0 and C_1 are obtained and therefore N_{DL} at a certain distance from the junction. Then, making a V_{DC} voltage ramp, the density profile of the net fixed charge (N acceptors – N donors) is obtained along the device (thus at different x_e) as shown in figure 5.9.

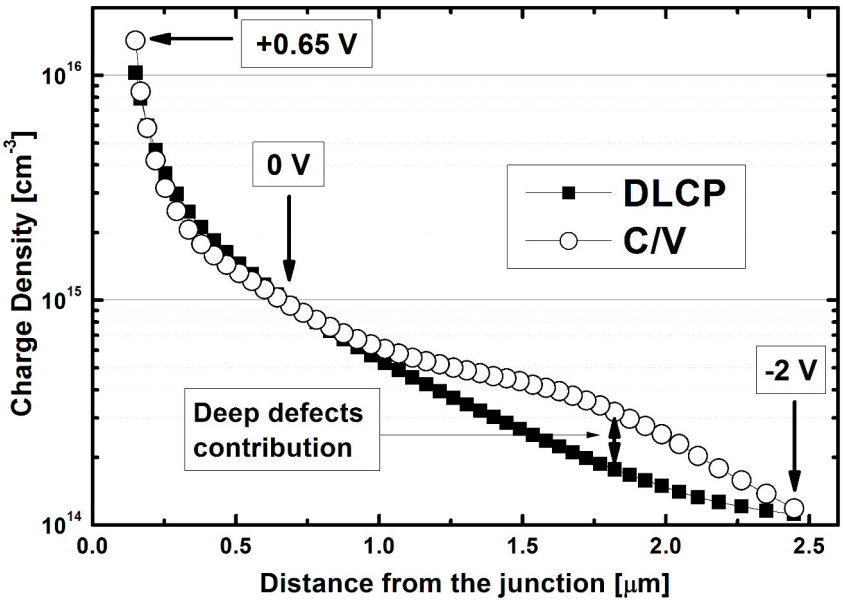

Figure 5.9: density profile of the net fix charge density Na-Nd along the device; comparison between CV and DLCP profiles [6].

To derive C_0 and C_1 the applied V_{AC} has to be asymmetric with respect to V_{DC} to shift both x_e and $x_e + \delta x$. V_{AC} is a sinusoidal signal that added to V_{DC} would move x_e between $x_e + \delta x$ and $x_e - \delta x$. Thus to keep x_e as the lower limit of the oscillation (as shown in figure 5.10), each time that V_{AC} is increased, V_{DC} must be decreased of the same value; in that way the maximum voltage applied V_{MAX} is constant.

$$V_{AC1} + V_{DC1} = V_{AC2} + V_{DC2} = V_{AC3} + V_{DC3} = \ldots = V_{MAX}$$

This ensures that all the capacitance measurements, done to obtain the curve from which C_0 and C_1 are extracted, refer to the same x_e.

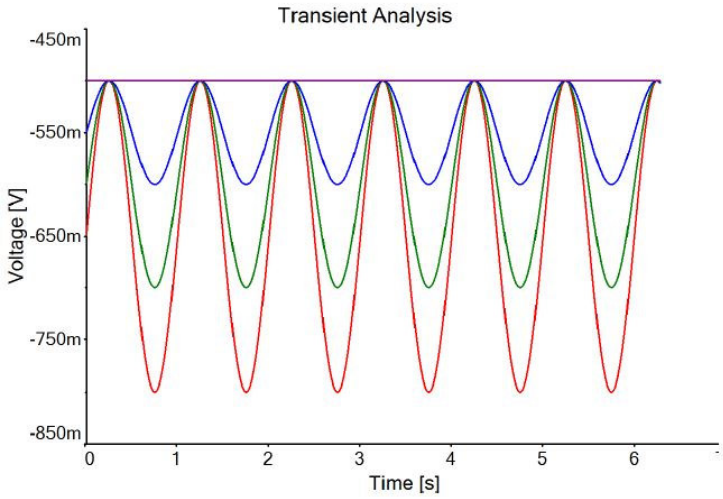

Figure 5.10: in the meanwhile that the amplitudes of V_{AC} are run, V_{DC} and V_{AC} are varied simultaneously to maintain constant the position of x_e [7].

5.4 Admittance spectroscopy (AS)

Once the information on the amount of deep and shallow defects have been obtained through CV and DLCP, the admittance measurement represents an important step for the complete electrical characterization of the device as it allows to identify the nature of the dominant defects.
As already mentioned talking about CV measurements, the defects can be "slow" or "fast" to respond to the electrical signal at different frequencies. Based on this consideration, the variation of the capacitance of the device as a function of the frequency is measured. In this way, not only the actual existence of the defect is highlighted, but it can also be characterized according to the response frequency.
The capacitance value in the first part of the curve in figure 5.11 indicates that most of the defects respond to the electrical signal, being part of the charge stored in the device. Increasing the frequency, gradually the slower defects stop following the signal. A very steep step indicates the presence of defects with similar response times. On the contrary, a less steep step indicates defects that respond to frequencies over a wider range, and therefore probably of different nature. The value of the capacitance at low frequencies, when all the defects are able to respond, gives an idea of the density of defects in the crystal.

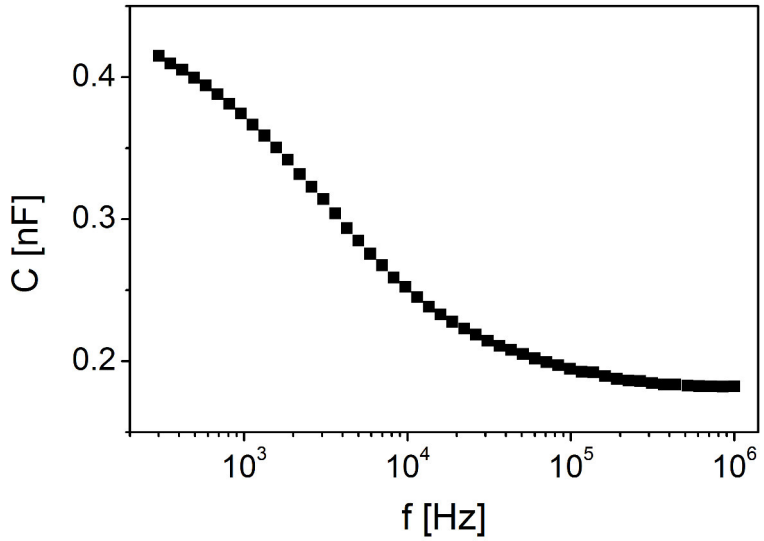

Figure 5.11: capacitance-frequency curve.

This measurement is then repeated at different temperatures. The obtained CF curves show a constant shape, but they are translated along the axis of the abscissas (as shown in figure 5.12). In particular, as the temperature increases, the curve moves to the right so that the measured values at low temperatures and low frequencies coincide with the measured values at high temperatures and at high frequencies.

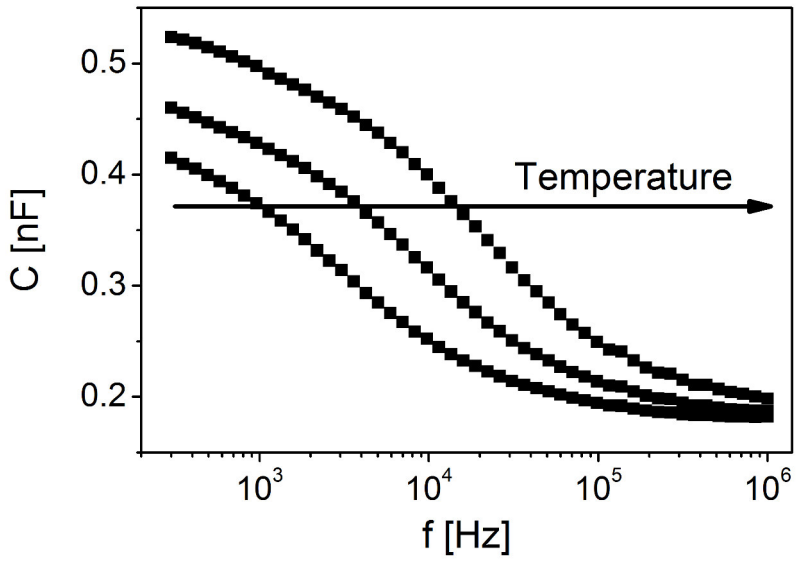

Figure 5.12: CF curves obtained at different temperatures: as the temperature increases the CF curve translates to the right.

At higher temperatures, a larger number of defects is able to respond to higher frequency signals; in fact, the defects are more reactive as the lattice vibrations increase.
In the case of a single dominant acceptor defect with energy E_t (above the valence band) and with characteristic frequency ω_t, where [8]:

$$\omega_t = \frac{1}{\tau_t} = e_p + c_p$$

$$e_p = N_v(T) < v_{th} > \sigma_p e^{-\frac{E_t - E_v}{kT}}$$

$$c_p = N_v(T) < v_{th} > \sigma_p e^{-\frac{E_F - E_v}{kT}}$$

and e_p and c_p are the emission and the capture rate of the defect, respectively, and

$$v = N_v(T) < v_{th} > \sigma_p$$

is the thermal emission coefficient, and it depends on the actual density of the states in the valence band N_v, on their average thermal velocity $<v_{th}>$, and on the capture cross section σ_p of the involved defect. It is important to underline that E_t and σ_p, which are considered independent of temperature, are enough to determine ω_t.

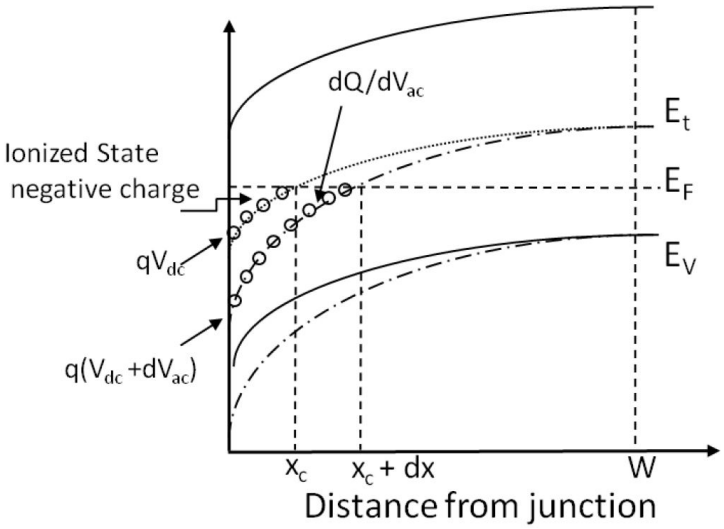

Figure 5.13: contribution of deep defects due to the application of V_{AC} [6].

Referring to figure 5.13 above:

- in x_c, called crossing point, $E_F = E_t$ then $e_p = c_p$; this implies that the amount of electrons that is captured by the traps is equal to the amount that is emitted.
- in $x < x_c$, $E_t < E_F$ and $c_p > e_p$; therefore the traps are mainly occupied (ionized charges).
- finally in $x > x_c$, $E_t > E_F$ and $c_p < e_p$; so most of the traps are unoccupied (neutral charge).

Practically, to determine ω_t the capacitance is measured by scanning the frequencies of a small amplitude V_{AC} signal, at a fixed temperature and a fixed voltage V_{DC}. The latter determines the bands bending and therefore x_c.

When $\omega_{AC} < \omega_t$ the charges can be captured and emitted, while when $\omega_{AC} > \omega_t$ the charges are not fast enough to follow the alternating signal, and the capacitance is influenced only by the V_{DC} signal.
When a dominant deep defect responds to V_{AC}, the Admittance measurement presents a curve like the one in figure 5.14:

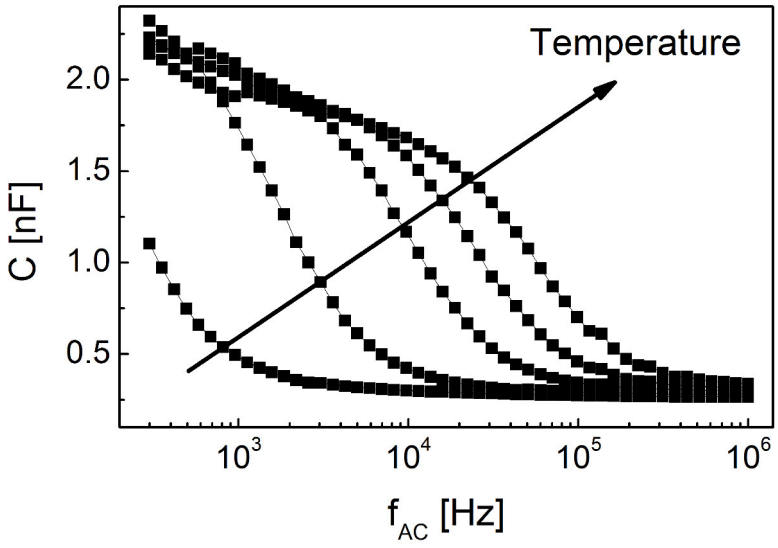

Figure 5.14: AS curve at different temperatures in the presence of a dominant deep defect [6].

By differentiating it can be plots $-f_{AC}\frac{dC}{df_{AC}}$ as a function of the frequency f_{AC}, where $\omega_{AC} = 2\pi f_{AC}$,

in this way the peak reveals the ω_t of the defect (figure 5.15) [7].

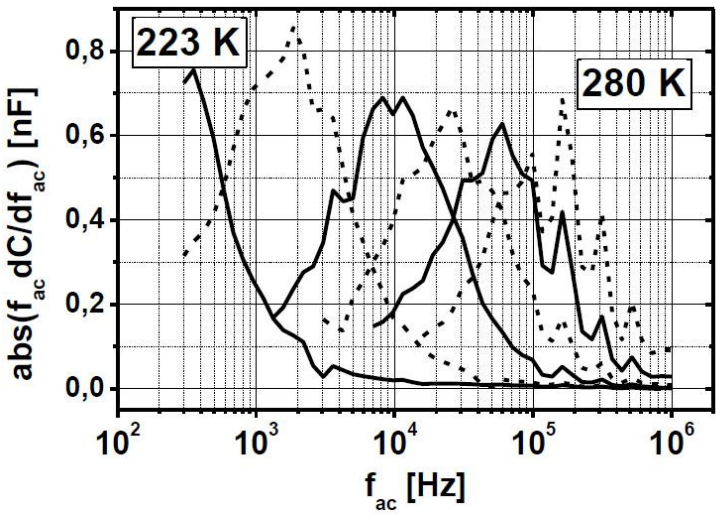

Figure 5.15: the peak reveals the ω_t of the defect at different temperatures [6].

So at the crossing point x_c, it can be written:

$$\omega_t = 2e_p = 2\nu e^{-\frac{E_t - E_v}{kT}}$$

Dividing by T^2 and solving the equation:

$$\ln\frac{\omega_t}{T^2} = \ln\frac{2\nu}{T^2} - \frac{E_t - E_v}{kT}$$

By changing the temperature and repeating the measurement, the peak moves; in this way the Arrhenius graph is drawn (figure 5.16):

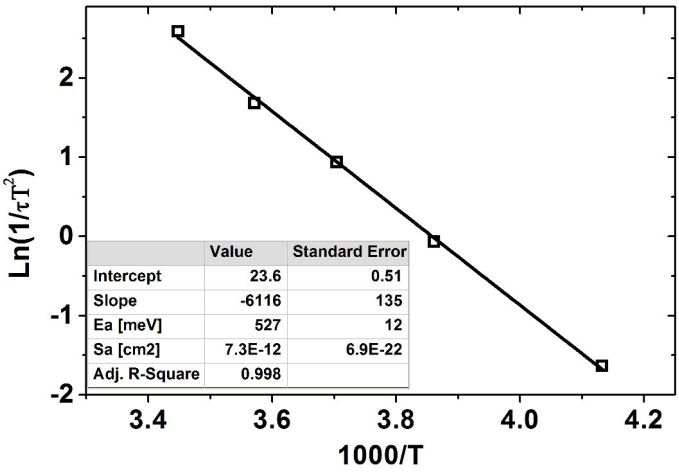

Figure 5.16: Arrhenius graph obtained from the AS measurement performed at different temperatures [6].

Through the linear interpolation of this graph it is possible to calculate σ_p from the intercept and E_t from the slope.

5.5 References

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6
Study of alternative window/buffer layer

6.1 Thin CdS treated buffer layer

CdTe-based solar cell has demonstrated to be so far one of the best thin film photovoltaic technologies, reaching laboratory conversion efficiencies of more than 22% [1]. One of the major improvements for CdTe solar cells is the increase of the current density by increasing the transparency of the buffer layer. CdS, with its 2.4 eV band gap, results to be opaque at low wavelength regions. For this reason, in order to gain in blue and UV light, extremely thin CdS has to be applied, if the buffer is not substituted with other materials. Historically, the best way to reduce CdS thickness is given by chemical bath deposition, where the polycrystalline layer is formed by precipitation of the material on the TCO/glass stack. This allows a larger range of thicknesses; anyway, not below 80 nm, where ultra thin CdS layer delivers shunts with a large reduction of fill factor and open circuit voltage, despite the increased current density. In fact it is well known that a reduced amount of CdS would consume into the CdTe, giving place to a direct contact between CdTe and transparent conductive oxides (TCO).
To solve this problem, we have systematically reduced the thickness of CdS, prepared by thermal evaporation in vacuum, from our standard 150 nm thick layer to very low thickness values: from 80 nm down to 30 nm. Moreover, we have introduced a post deposition treatment by chlorine-containing gas on the CdS layer at high temperature, in order to stabilize the layer and avoid shunts. Then we have compared it with annealing treatment at same temperature and time but in a pure Argon atmosphere and with standard vacuum annealing process at 450 °C. The thin CdS layers annealed with the chlorine treatment performed improved open circuit voltage of the finished devices.
In this chapter a study of treated thin CdS with recrystallization treatments is presented; the layers have been analysed by means of X-ray photoelectron spectroscopy, X-ray diffraction and atomic force microscopy. Finished CdTe devices made on thin CdS are characterized in terms of current-voltage and quantum efficiency.

6.1.1 Experimental procedure

In our lab, CdTe solar cells are typically fabricated in superstrate configuration. On a a 3x3 cm^2, 4 mm thick, soda-lime glass a stack of 400 nm thick indium tin oxide (ITO) film is deposited by RF-magnetron sputtering with 90% In_2O_3 and 10% SnO_2 target (99.99% pure) in Ar + 2% O_2 atmosphere and with a substrate temperature of 400°C. Then the front contact is completed by covering the ITO layer with a 100 nm thick i-ZnO film, deposited by RF magnetron sputtering from a 99.99% pure ZnO target in atmosphere of Ar+2% O_2 and at a substrate temperature of about 400°C. CdS layer is deposited on the ITO/ZnO stack by high vacuum thermal evaporation with a deposition rate of 1 nm per second and a pressure of 10^{-4}

Pa (no significant changes are registered before and after deposition), where the substrate is kept at 150°C. Typically, CdS thickness is around 150 nm and after deposition the layer is annealed in vacuum at 450 °C. In this work the CdS preparation is different in thickness and in post deposition treatment compared to the above-mentioned standard process. More details will be reported in the next section.
CdTe film is deposited by thermal evaporation in the same CdS vacuum chamber with a deposition rate of 20 nm per second, at a pressure of 10^{-4} Pa (no significant changes are registered before and after deposition) and a substrate temperature of 340°C and with a thickness of about 5-6 microns. Subsequently, CdTe is activated with a solution of $CdCl_2$ in methanol, applied on the CdTe surface and by annealing the stacks in air at 380 °C for 30 minutes. Prior to the back contact, CdTe is etched in a Br-methanol solution, promoting the formation of a p^+ Te rich layer on the CdTe surface. Finally the back contact is produced by depositing a 2 nm thick Cu and a 30 nm thick Au films by vacuum evaporation at room temperature and the finished device is annealed in air at 190°C for 20 minutes.
All the temperatures measured in the deposition machines and in the furnaces are actual values measured with thermocouples inserted in the substrate holders.
The transmission and band gaps of CdS layers have been analysed by a Unicam spectrometer Type UV2-100 in UV-visible range; their morphology and roughness by NT-MDT atomic force microscopy Solver-Pro with NT-MDT NSG01 golden silicon tips in semi-contact mode. CdS stoichiometry was measured at Department of Physical and Chemical Sciences, University of L'Aquila, by X-Ray Photoelectron Spectroscopy: PHI mod. 1257 equipped with a non-monochromatic twin anode (Al/Mg) X-ray source (Mg anode has been used, E=1253.6 eV) and a hemispherical analyser. The crystalline structure was studied by using a Siemens D5000 system, with Cu anode (λ=0.15604 nm) and equipped with Göbel Mirrors (to obtain a parallel X-ray beam, divergence lower than 0.03°). Current density-voltage characteristics of the completed cells were measured with a Keithley Source Meter 2420, two probe contact, using a halogen lamp calibrated with a silicon solar cell under an irradiation of 100 mW/cm^2. Finally external quantum efficiency measurements have been performed at Department of Information Engineering, University of Padova, with a commercial LOANA (PV-Tools GmbH) solar cell analysis system,. The EQE measurements were calibrated with a silicon reference sample with known response using an incident spotlight of 1mm x 2 mm area.

6.1.2 CdS post-deposition treatment

Only recently high efficiency CdTe solar cells without CdS buffer layers have been fabricated [2, 3] by the application of magnesium zinc oxide combined with the insertion of CdSe into the first layers of CdTe, near the junction. Anyhow CdS still is one very good option for high performing junction with CdTe.
However, as already mentioned, this material suffers of a low band-gap, which results in cutting wavelengths in the range of 400-500 nm [4]. To mitigate this drawback there have been many attempts in the direction of reducing CdS thickness and to improve the light transmission in this wavelength range. Fabricating a thin layer with good conformal coverage by physical vapor deposition is more complicated. Best results have been obtained by chemical bath deposition [5, 6], but it has some limitations for industrial application. Moreover the pinholes in these thin CdS layers were controlled by high resistive transparent layer such as, for example, zinc stannates [7].

Another possible alternative solution to this issue is to implement CdS in order to improve its transparency; possible paths include to add impurities to enlarge the band gap, such as for example oxygen or fluorine [8, 9] or alloying the CdS with ZnS [10].
The low thickness results to be detrimental also because even in case the CdS is uniformly deposited, it can be consumed in CdTe after $CdCl_2$ treatment, since the activation enhances intermixing of CdS into CdTe forming a CdS_xTe_{1-x} intermediate layer [7, 11, 12].
Generally when an excess of CdS consumption in CdTe is observed, the solution is to tune the $CdCl_2$ treatment mainly by reducing the annealing temperature. However this limits the optimum activation of the CdTe layer [13, 14]. In this work we decided to go upstream and to reduce this interdiffusion by improving the CdS stability, this would allow to obtain a thinner CdS layer without the formation of pinholes after $CdCl_2$ treatment.
In our laboratory, the CdTe solar cell fabrication process, that delivers efficiencies between 14 and 15% [15], includes annealing of the typical 150 nm thick CdS layer at 450° in vacuum prior to the CdTe deposition, which is crucial for tuning the CdS/CdTe interface.
We have prepared thin CdS layers that, after deposition on the TCO/glass stack, are treated with a chlorine containing gas. The insertion of chlorine is expected to recrystallize the CdS layer, as it typically does for CdTe. In details this process, named as "DFC-treated", consists in annealing at 550 °C at a pressure of 10^3 Pa in Argon atmosphere for 30 minutes and in additional $0.5*10^3$ Pa of difluorochloromethane (chlorine-containing gas) for the last 5/10 minutes,.
The idea is not completely new, studies of $CdCl_2$ treated CdS for CdTe solar cells have been already made, actually without improving efficiency [16]. However in this work we combine the recrystallization process to stabilize the CdS layer by chlorine containing gases with the thinning of vacuum evaporated CdS layer.
Also two additional annealing processes (see table 6.1-I for a schematic list) are taken in consideration for comparison. The first is our standard process: CdS annealing at 450 °C for 30 min at a pressure of 10^{-4} Pa [17], named as "reference". The second , named as "AR-treated", consists in a CdS annealing at 550 °C for 30 minutes at a pressure of 10^3 Pa of Argon, which avoids re-evaporation of CdS at high temperature. It is applied just to highlight the effect of high temperature without the chlorine influence; this is very important to discern between temperature and chlorine effects.
The ultra thin treated CdS layers will be analyzed as follows and the respective solar cells will be measured.

Table 6.1-I. List of the different CdS annealing processes taken into account.

Name	Temperature (°C)	Time (min)	Pressure (Pa)	Atmosphere	Chlorine
Reference	450	30	10^{-4}	Vacuum	
AR-treated	550	30	10^3	Argon	
DFC-treated	550	30	10^3	Argon	$0.5*10^3$

6.1.3 Solar cells performance

Table 6.1-II. Average efficiency parameters of solar cells with differently treated CdS films with standard deviation (16 cells for each treatment were considered).

CdS_treatment	$V_{oc}\pm\Delta V$ (mV)	$J_{so}\pm\Delta J$ (mA/cm^2)	FF±ΔF (%)	η±Δη (%)
Vacuum annealed	780 ± 8	26.0 ± 1.0	62.8 ± 1.7	13 ± 0.5
DFC-treated (5 min.)	800 ± 13	26.5 ± 1.3	62.7 ±1.5	13.5 ±1.0
DFC-treated (10 min.)	670 ± 4	26.1 ± 1.0	63.7 ± 0.5	11.7 ± 0.4

Finished devices have been fabricated with CdS layers treated according to the three different recipes stated in the previous chapter. The performance shown in table 6.1-II belongs to devices made with 30 nm thin CdS layers. Moreover, particularly for comparing the gain in the low wavelength region in respect to thicker buffer layers, EQE analysis was made on cells with an area of 0.135 cm^2 (measured with Zeiss Axio-vision microscope equipped with computer interfaced digital camera) made with 30 nm and also with 80 nm thick CdS layers. Obviously we expected that a progressive reduction of CdS thickness would result in an increase of the current density and a progressive decrease in open circuit voltage and fill factor.

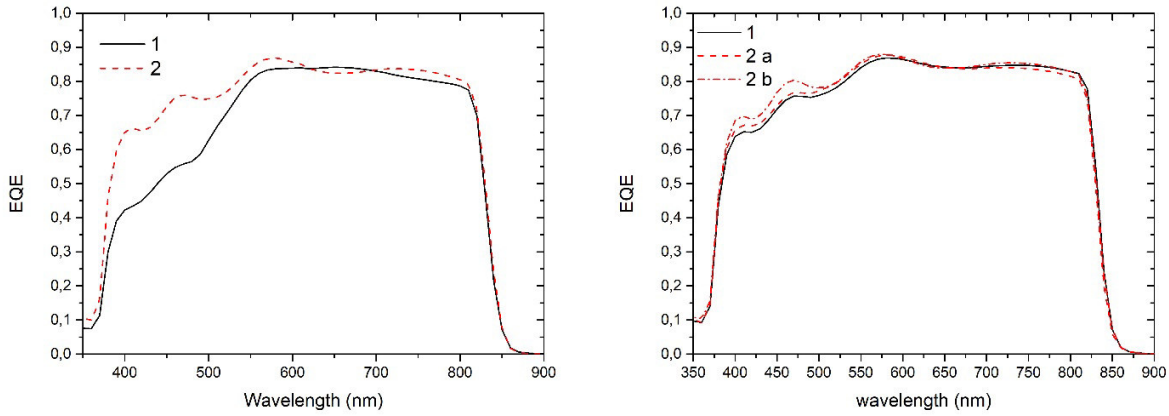

Figure 6.1.1: EQE of CdTe devices fabricated with (left) 80 nm CdS: 1) vacuum annealed and 2)10 minutes DFC-treated. 30 nm CdS (right) treated with 1) vacuum annealing, 2a) 10 minutes DFC treatment 2b) 5 minutes DFC treatment

In figure 6.1.1 EQE measurements of devices made with differently treated and thick CdS are shown (please take in consideration that data are not referred to record cells and that spectral response is relative). The DFC treatment performs an increased response for ultra thin CdS layers at the low wavelength region, attributable to CdS.
The DFC-treatment at 30 nm is successful, but only when chlorine is applied for 5 minutes. If the treatment is prolonged to 10 minutes, a lower performance is observed. This increased performance is generated from Voc and Jsc increase, shown in table 6.1-II, but for different reasons. In particular, the current density improves mainly for the reduction of CdS thickness

(30 nm); this is demonstrated by the fact that similar current densities are obtained for reference and DFC-treatment. However when the DFC treatment time is optimized, open circuit voltage is higher compared to devices with vac-annealed CdS (see table 6.1-II and figure 6.1.2), thus the Voc gain is due to the presence of chlorine.

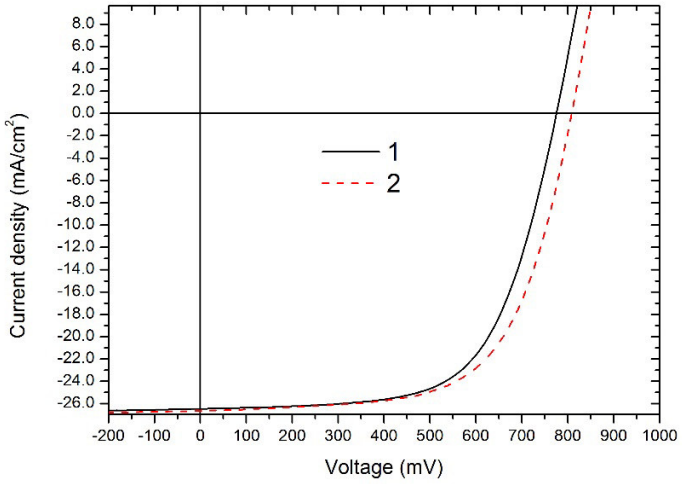

Figure 6.1.2: I-V curves of the best V_{oc} cells with 30 nm CdS: 1) Vacuum annealed and 2) 5 minutes treated

6.1.4 Analysis

In order to understand if the different post deposition treatments influence the transparency of the CdS layer, transmittance measurements were made on a set of samples and the band gap was determined by the Tauc plot procedure [18].
In order to differentiate the effect of temperature (from 450 °C to 550 °C) from the effect of chlorine on the CdS, transmittance measurements (and their according calculated band gap) were carried out on three different samples: 1) reference 2) AR treated 3) DFC treated. Number two and three were made at same temperature and pressure for the same time.
The different CdS layers do not show a prominent increase in transparency; only a slight increase at the low wavelength region below 400 nm is registered. However a slight change in the band gap is observed: annealing shifts the band gap at higher values, in particular DFC-treatment is slightly more effective in this sense (see Table 6.1-III: values are precise to the last digit (+- 0.01 eV)).

Table 6.1-III: Band gap values extracted from the Tauc plot and difference before and after annealing (last column).

CdS treatment	Before ann. (eV)	After ann. (eV)	ΔE (eV)
Vacuum annealed	2.29	2.30	0.01
Argon annealed	2.28	2.33	0.05
DFC-treated	2.29	2.35	0.06

Argon treated CdS layers has however provided lower efficiency with very low open circuit voltage values (in the range of 670 mV), for this reason we do not report here analysis of these layers (even if they were actually processed). However this proves that not only high temperature but also the presence of chlorine improves efficiency for thin CdS layers. Generally, annealing a thin film at much higher temperatures than deposition temperature delivers an enhancement of the grain size and an improvement of the crystal quality. In our case just by annealing the layer at 550 °C and we did not notice large changes in the morphology.

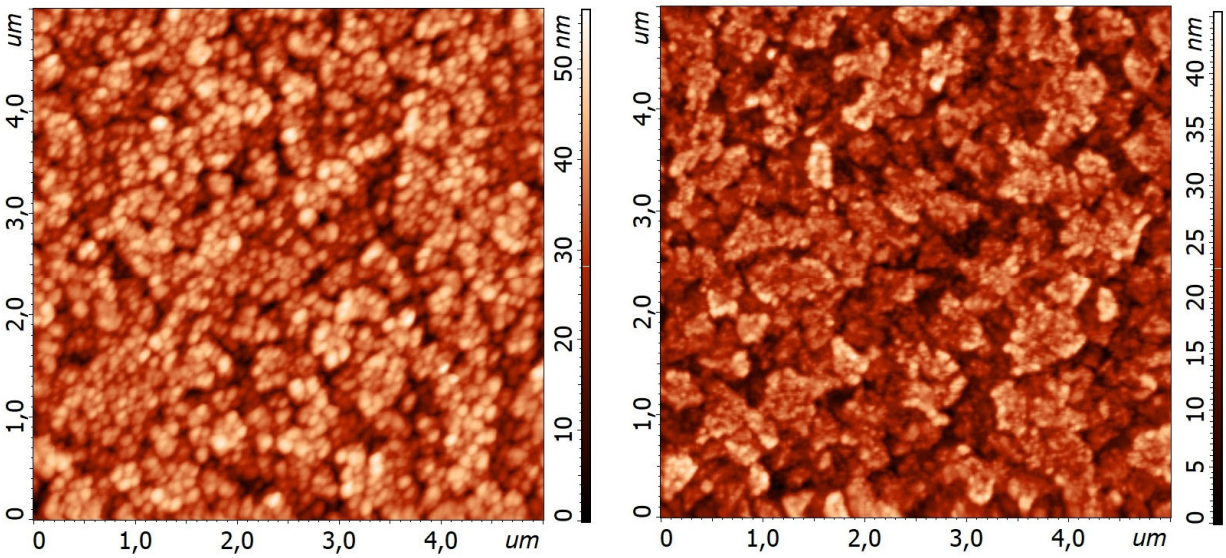

Figure 6.1.3: AFM pictures of CdS after reference and DFC treatment

Table 6.1-IV: Roughness comparison of reference and DFC treated CdS layers.

Sample	Peak to peak (nm)	Root Mean square (nm)	Average (nm)	Average roughness (nm)
Reference	54.41	8.00	29.32	6.35
DFC-treated	42.93	6.02	20.28	4.74

From the analysis of the AFM data of the reference type and of the DFC-type samples, we observe that chlorine smooth the sample surface (see table 6.1-IV). Moreover a slight recrystallization of the grains is observed after DFC-treatment,: the poly-crystals form larger clusters (see figure 6.1.3).

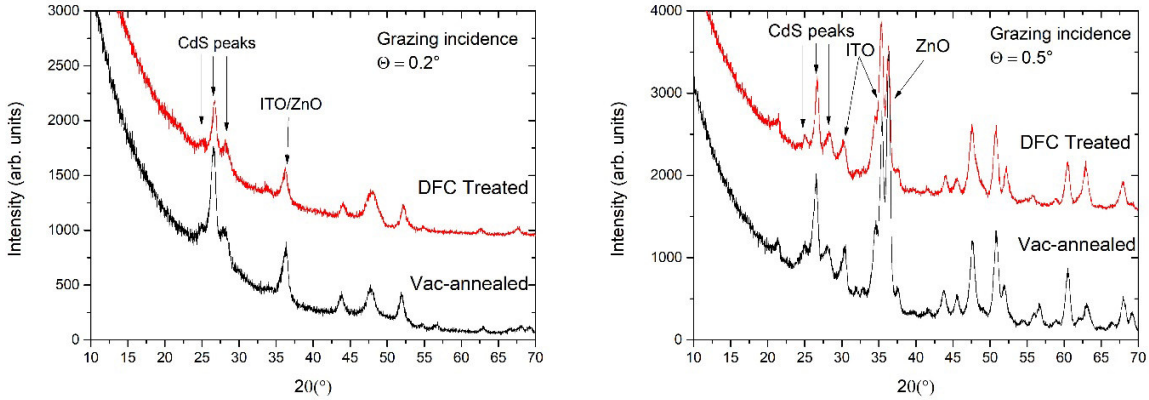

Figure 6.1.4: GXRD spectra at 0.2° and 0.5° grazing angle of CdS, vacuum annealed and DFC-treated

A more accurate indication of the possible recrystallization is given by XRD patterns, which were applied on the reference and the DFC type samples.
Due to the reduced thickness of the CdS, the contribution of the ZnO substrate and of the ITO is largely present in the pattern and it complicates the attribution of the peaks to the CdS. For this reason grazing angle XRD have been processed at different angles: 0.1°, 0.2°, 0.5°, 1°, 2°; in figure 6.1.4 only GXRD patterns at 0.2° and 0.5° are shown.
In figure 6.1.4, the XRD patterns do not show significant variations of the CdS peaks registered between the differently treated layers. Only a slight shift between the expected CdS peaks and the measured ones is observed.
The main three peaks in the range between 25-28 ° all correspond to CdS, while the peak positioned at 35° is given by the overlap of a ZnO peak and of an ITO peak.

By now we have observed that DFC treatment actually only very slightly changes the band gap of the CdS. Moreover only a slight reorganization of the grains is observed in the morphology (AFM pictures not shown here). In order to verify if any change in the chemical structure of the layers is generated, XPS have been made on CdS/ZnO/ITO stack annealed according to three different processes mentioned above (see figure 6.1.5).

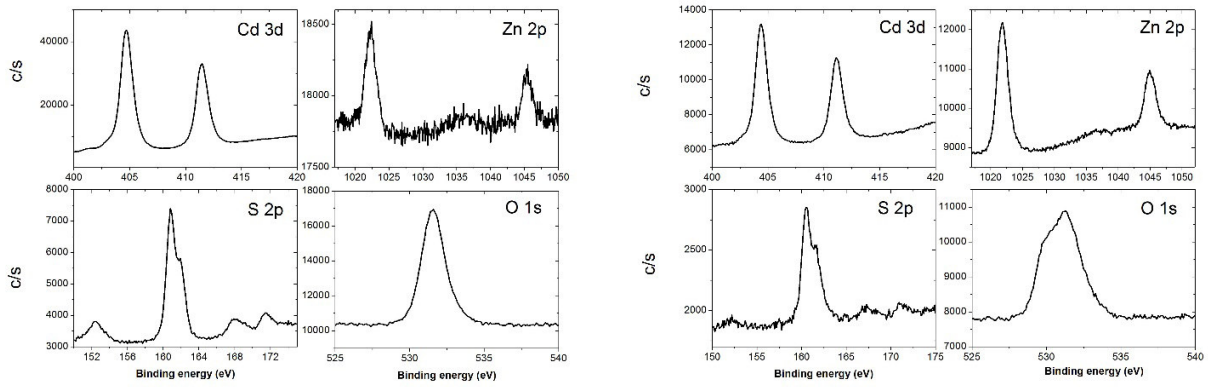

Figure 6.1.5: XPS of CdS on ZnO/ITO coated glass substrate, annealed in vacuum (left) and annealed in DFC-atmosphere (right)

The main peak of C1s carbon at 284.50 eV was set for the analysis. A very small trace of chlorine is observed for all samples, with no difference between reference and DFC-treated CdS, showing that DFC-treatment does not actually leave any additional chlorine on the layer. On the other hand in all the samples peaks of S, O, Cd and Zn are shown (figure 6.1.4). The signals of the Cd and S (in shape and width) are superimposable (the full width at half maximum FWHM for Cd is about 1.24 eV in both vacuum and DFC annealed, while for S the FWHM is 1.93, again for both samples), so only one phase, CdS, is observed. Regarding the concentrations: the calculated ratio of the peak areas (Cd 3d 5/2 / S 2p) is 7.3 for vacuum treated CdS whereas it is 5 for DFC treated ones. Calculating the atomic concentrations from these data, Cd/S ratio is 1.27 for reference and 0.87 for DFC-treated, however the error calculation is large enough (20%) to state that stoichiometry is very similar with a slightly less cadmium concentration observed for DFC treated samples, and this might be coherent with the reduction in Cd binding energy (a shift of about 0.2 eV) for the DFC-treated case. Regarding ZnO: the difference in energy of the peaks 2p between metallic Zn and oxides is very small (0.1-0.1 eV), so we can refer exclusively to the presence of oxygen. Typically, the presence of ZnO gives rise to a second peak (in addition to that of native oxygen for exposure of the sample to air) to an energy of about 530 eV [19], compatible with the O 1s spectrum observed in the DFC-treated sample, while for reference sample the shoulder in the O 1s cannot be seen (see figure 6.1.4, O 1s). It is evident that the zinc signal in the left spectrum (the reference sample) is much smaller than the right one (DFC-treated sample) (700 c/s vs. around 3000). On the other hand, the presence of ZnO is established by the presence of the second peak in oxygen, rather than the shift in energy of the Zn 2p, which is very small. If for the reference sample no zinc oxide is observable, together with the very low Zn signal, it means that the Zn detected is the one below the Cd film and therefore it is not oxidized.
This states that no ZnO is observed for reference sample as expected (XPS analyses surfaces with depths not larger than 5 nm), but it is present on the surface of CdS when it is DFC-treated.
As far as stoichiometry is concerned, the samples have substantially the same composition, but slightly different thicknesses.

The presence of ZnO signal could be explained as the tendency of the DFC-treatment to remove weak bonds in CdS leaving space to ZnO. In this sense DFC-treatment would have the role to improve the stability of CdS, explaining the higher open circuit voltage of the devices with thin buffer layer.

6.1.5 CdTe growth on differently treated CdS

In order to understand the effect of the differently treated CdS layers on CdTe, XRD have been performed on CdTe grown on the differently treated CdS. CdTe peaks (see figure 6.1.6) present very similar intensity and position demonstrating a very similar crystallization of the absorber, independently of the treatment of the CdS.

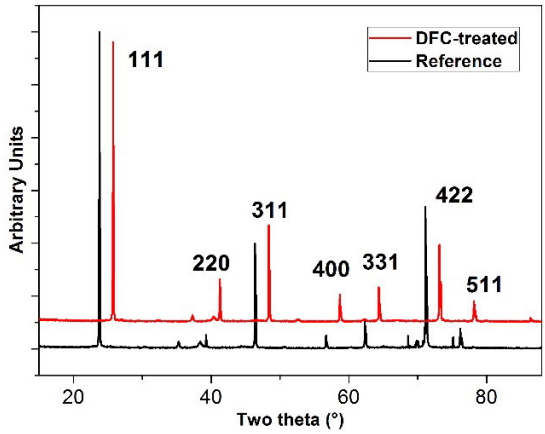

Figure 6.1.6: XRD of activated CdTe on vacuum annealed CdS (Reference) and DFC-treated CdS

Applying the well-known calculation, usually called Nelson-Taylor plot, which allows to extract from the position of the different peaks the lattice parameter in a cubic structure [20, 21], we have obtained the different values according to the different CdS layers. CdTe lattice parameter results to be 6.487 Å for DFC-treated layer against 6.488 Å for vacuum annealed. Since the difference is very small and within the error (0.001 Å) we can conclude that the intermixing of the CdS/CdTe junction is similar for both cases.

6.1.6 Discussion

Solar cells with thin CdS layers are affected by micro-pinholes resulting in lower open circuit voltage, as observed also from our experiments. When CdS is treated with difluorochloromethane, the finished devices perform a net higher Voc, but similar current density and fill factor.
Moreover a net higher response in the low wavelength region is observed when chlorine is applied. The effect of chlorine is demonstrated by the fact that annealing at same temperature and pressure in pure argon does not provide improvement, on the contrary a net reduction of open circuit voltage is observed.

We have analysed the crystallization of the grains, after chlorine treatment, in terms of morphology, but very slight change is observed. A very small enlargement of the grain size and a smoother surface occur.
XPS analysis basically demonstrates that no change in CdS stoichiometry appears after DFC treatment, however ZnO is observed on the CdS surface and this ZnO-CdS mix could be the explanation for the increase in the CdS band gap.
CdTe changes slightly in terms of structure, morphology and lattice path, and it can be concluded that no change in the junction has been obtained.

6.1.7 Conclusions

Very thin CdS layers for CdTe solar cells have been prepared and treated in vacuum, argon and with a chlorine containing gas, at temperatures up to 550°C.
After DFC-treatment, AFM images show an increased smoothness of the layers without losing in thickness, and a different rearrangement of the crystals. XPS shows that DFC intermixes CdS and ZnO layers; this is also confirmed by the increased transparency and improved performance of the solar cell.
DFC-treated ultra thin CdS layers deliver devices with high current density and high open circuit voltage at the same time. Most probably the process protects the device from shunting, due to the larger grain size and the slight mix of CdS/ZnO layers.
Treatments at temperatures above 500 °C in argon and chlorine atmosphere on 80 nm thick CdS have led to the fabrication of more stable samples compared to not treated CdS, resulting in improved performance with a 10% increased current density and a 5% increased open circuit voltage and fill factor. Moreover, light transmission of the CdS treated layers from 300 to 450 nm is increased of about 10%.
We have introduced an original treatment for CdS layer, which allows reducing considerably the thickness of CdS, reducing the open circuit voltage loss.

6.1.8 References

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6.2 Introduction of MgZnO as a high resistivy transparent buffer layer

CdTe solar cells are manufactured on a large scale and with high efficiency by vapor transport deposition (VTD) with a record cell efficiency exceeding 22% [1]. VTD together with Close Space Sublimation has delivered the highest efficiencies using high substrate temperature avoiding re-evaporation of the material. It is known that high substrate temperatures result in large grain size with a reduced number of grain boundaries and this is believed to contribute to the high efficiency. However, use of high temperature requires robust substrates and excludes the use of most flexible substrate materials. It also involves higher energy consumption and more complicated machinery.
Although no explanation has been provided for the high current density produced in the champion cell, it is speculated that the junction has been optimized by the reduction of absorption in the CdS as well as optimization of the back contact with a back reflector. Back contacts as ZnTe:Cu have been introduced since the beginning of the 2000s [2]. 16.7% efficiency by VTD has been obtained by inserting a Cd_2SnO_4 as transparent conductive oxide (TCO) and a Zn_2SnO_4 high resistance transparent (HRT) layer. High efficiency devices exceeding 18% were presented by Sites et al. [3] by introducing a MgZnO buffer layer and other improvements including a broadband antireflection coating and a Te compound as a back reflector.
In the work presented in this chapter, we have studied the introduction of a Mg doped ZnO HRT layer to replace our standard insulating ZnO layer. ITO/MZO layers were fabricated at Loughborough with different substrate temperatures and their physical properties have been studied. Finished solar cells have been fabricated on the prepared TCOs and physical and electrical properties have been analyzed.
Devices show different performance according to the different substrate temperature deposition. A larger amount of Mg results with higher substrate temperature and consequently a higher band gap is registered. This optimized process has delivered solar cells with efficiencies up to 16.2%, which is one of the highest reported for substrate temperatures below 500°C.

6.2.1 Experimental procedure

At Loughborough University, Indium-doped Tin Oxide and Mg doped ZnO thin films were deposited on soda lime glass by Radio-Frequency (RF) magnetron sputtering. The films were deposited using an Orion 8 HV magnetron sputtering system (AJA international, USA) equipped with an AJA 600 series RF power supply. The 3” diameter ITO target (90% In_2O_3 and 10% SnO_2, 99.99% pure) and 3” diameter MZO target (11% MgO and 89% ZnO, 99.95% pure) were rotated at 10 rpm during deposition to assure uniformity. Both targets were sputtered at a constant power density of 3.5 Wcm^{-2} and at an Argon pressure of 133.3 Pa. 1% O_2 in Ar atmosphere was added for the MZO deposition. Substrate temperature was

set to 450 °C for ITO deposition, while for MZO deposition substrate temperatures from 20 °C up to 400 °C were applied.
At the University of Verona the ITO/MZO substrates were coated with CdS and CdTe by thermal evaporation in a vacuum chamber at a pressure of 10^{-4} Pa with a Edwards XDS10 roughing pump and a Edwards ST-451turbo-molecular pump. CdS is evaporated from a tungsten crucible at a deposition rate of 5 Å/sec. During deposition the substrate was kept at 150 °C with halogen lamps. Before and after CdS deposition, the stack is annealed in vacuum at 450 °C for 30 minutes, this allows the polycrystals of ITO/MZO and the deposited CdS to crystallize and increase robustness for the depositions and treatments that follow. CdTe was deposited from a special graphite Knudsen cell at an evaporation rate of 10 Å/sec. The rate was controlled by piezoelectric quartz crystal with an Intellemetrics IL-150 controller. The CdTe activation treatment was carried out by deposition of $CdCl_2$ in methanol solution. This is prepared by dissolving the $CdCl_2$ powder (previously dried in a furnace at 0.1 Pa) in methanol to form a saturated solution. The liquid is then deposited in the form of drops on the CdTe surface. A typical amount of 250 µl is calculated. Finally the stack is annealed in air at 380-400 °C for 30 minutes after a 25 minutes ramp from room temperature. The $CdCl_2$ treatment improves the electrical properties of the absorber (also by the passivation of the grain boundaries), enhances CdS/CdTe intermixing reducing the lattice mismatch and enlarges the grain size by one order of magnitude thereby reducing the density of grain boundaries [4]. In our laboratories we also have developed alternative activation treatment by application of chlorine containing compounds such as difluorochloromethane [5] or $MgCl_2$ (see chapter 7) [6]. However the $CdCl_2$ wet deposition delivers the highest performance.
The back contact consists of Cu/Au deposited on top of the CdTe layer, which was previously treated with a solution of bromine (50 µl) and methanol (40 ml) to clean the surface and remove $CdCl_2$ residuals to form a Te-rich layer. 2 nm thick Cu and 50 nm thick Au films were subsequently deposited by thermal evaporation at room temperature in a specific chamber with a vacuum of 10^{-3} Pa. Final annealing of the structure for 20 min at 190 °C in air, is necessary to obtain high efficiency.

The morphological properties of the CdTe layers were studied by atomic force microscopy (AFM) with a NT-MDT Solver Pro in semi-contact mode. X-ray diffraction analysis (XRD) of the CdTe layer has been performed by means of a Thermo ARL X'TRA powder diffractometer, operating in Bragg-Brentano geometry equipped with a Cu-anode X-ray source (Kα, k =1.5418 Å) and using a Peltier Si(Li) cooled solid state detector. Current density-voltage (JV) characteristics of the completed cells were measured with a Keithley Source Meter 2420, using a halogen lamp calibrated with a silicon solar cell under an irradiation of 100 mW/cm^2. Light transmission measurements of TCO layers were performed by a Unicam UV2 UV/Vis spectrometer. Finally external quantum efficiency measurements (EQE) have been performed at Department of Information Engineering, University of Padova, with a commercial LOANA (PVTools GmbH) solar cell analysis system. The EQE were calibrated with a silicon reference sample with known response using an incident spotlight of 1 mm x 2 mm area.

6.2.2 Results

Different solar cells have been prepared with MZO deposited at different temperatures. Bittau et al. have already observed that in these layers higher substrate deposition temperatures result in higher amount of Mg into the HRT layer; this provides a larger band gap and, consequently, a higher transparency [7]. Cells with MZO deposited at temperatures above 300°C have resulted in a superior conversion efficiency compared to the standard process with ITO/ZnO solar cells. Different annealing temperatures of the $CdCl_2$ activation treatment were applied to optimize the fabrication process. Most of the devices had superior efficiency, in the range of 14 % to 16 %. However, the best results were obtained by annealing the CdTe at 390 °C (as described above) and by a reduction of the CdS thickness to 100nm.
In Figure 6.2.1, the current density-voltage (JV) characteristic of a 16.2 % efficiency solar cell is shown
with a Voc= 852 mV, Jsc= 25,8 mA/cm^2 and a F.F.= 74 %. The parameters indicate a higher fill factor and current density, compared to our best ITO/ZnO devices (efficiencies are in the range of 15%) [8].

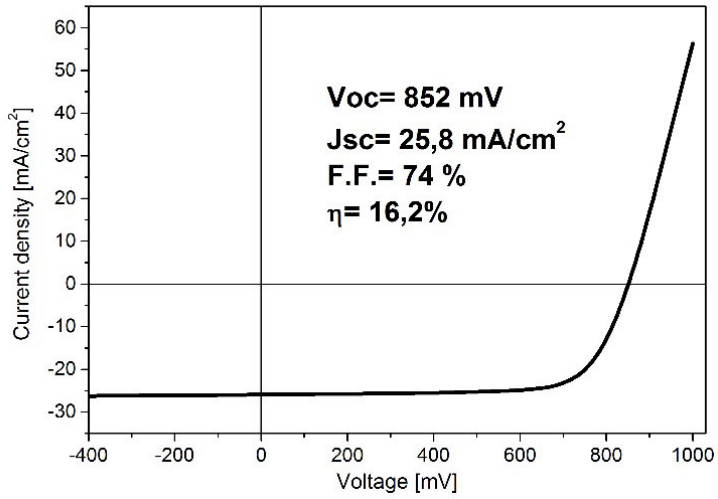

Figure 6.2.1: Current density-voltage characteristic of the highest efficiency CdTe solar cell with MZO/ITO front contact.

CdTe grown on CdS/MZO/ITO show a similar morphology irrespective of the MZO temperature and
slight different recrystallization (see figure 6.2.2). CdTe grain size is almost equal for the MZO (deposited at 200 °C and 400 °C) and for the ITO/ZnO cases. On the other hand, the orientation of the crystals shown on the XRD spectra slightly change their preferred orientation.

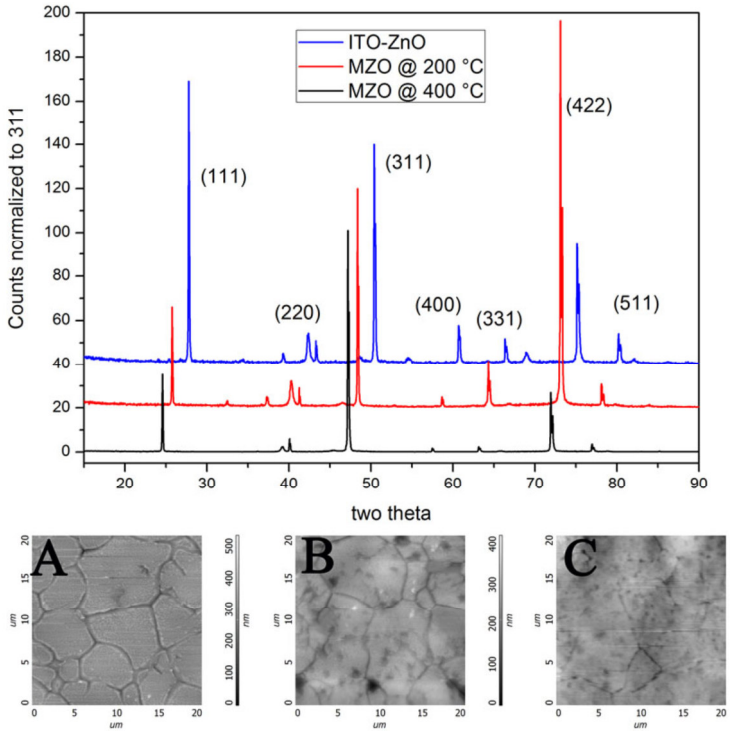

Figure 6.2.2: Comparison of XRD spectra of CdTe deposited on CdS and on ITO/ZnO or ITO/MZO (top) and morphology of CdTe deposited on CdS/ZnO/ITO (A), on CdS/MZO/ITO with MZO deposited at 200°C (B) and at 400 °C (C).

As already mentioned the application of MZO/ITO may result in higher transparency of the TCO layer (see figure 6.2.3). However, the improved performance is not entirely connected to an increased amount of photons absorbed in the CdTe.

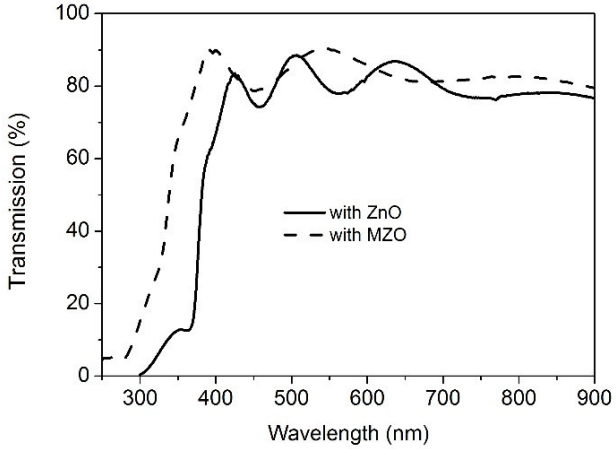

Figure 6.2.3: Comparison of transmission spectra of the new ITO/MZO stack with our standard ITO/ZnO stack.

In fact quantum efficiency measurement (shown in figure 6.2.4) shows a different response according to the different TCOs, and the insertion of the MZO layer improves the response across the entire wavelength range and in particular in the long wavelength region. This is not connected to a reduced absorption in the TCO and CdS layers.
It is possible to explain this phenomenon if we consider that the intermediate layer is not only preventing pinholes in case of ultra thin CdS layers, or limiting diffusion of impurities from the front contact [9] but also, as mentioned by Klein et al. [10], reducing the band offset between ITO and CdS.
Moreover Rao et al. have shown that MZO has a better lattice match with CdS compared to ZnO [11] and Kephart et al have demonstrated that it is even possible to tune the MZO band gap and electron affinity in a way to have an optimum match with CdTe, forming MZO/CdTe heterojunction [12].

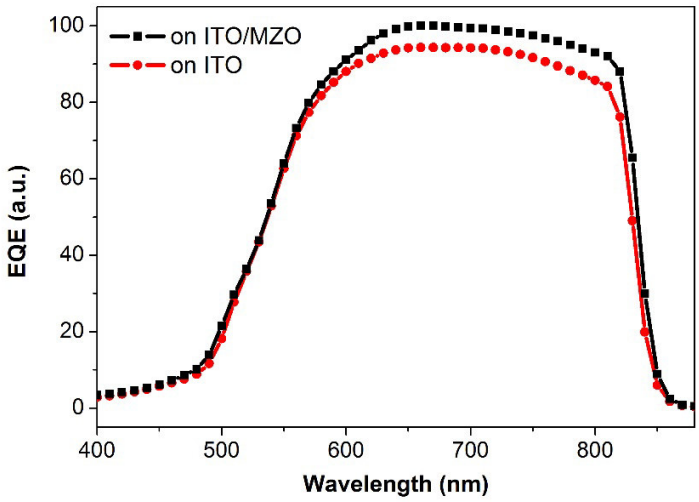

Figure 6.2.4: External quantum efficiency of CdTe solar cells made with only ITO and with ITO/MZO front contact (in this case CdS is thicker than record efficiency cells).

6.2.3 Conclusions

Thin film CdTe solar cells have been prepared using a low temperature substrate deposition process by
thermal evaporation in vacuum. The process has been optimized for a front contact with insertion of high resistance transparent HRT layer of Mg-doped ZnO. MZO substrate deposition temperature has been optimized in order to have the ideal band gap and produce a better match with the CdS buffer layer. Various $CdCl_2$ activation treatment temperatures have been used to optimize the fabrication process. The majority of devices have delivered high efficiency (from 14 to 16 %). The highest efficiency of 16.2% is a record for vacuum evaporated CdTe solar cells. The improvement of performance is not justified by the increased transparency of MZO but can be explained by an improved band alignment with the CdS buffer layer, compared to ITO or ITO/ZnO stacks.

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6.3 Introduction of MgZnO as a window/buffer layer

I have already shown that Magnesium Zinc Oxide (MZO), deposited by RF magnetron sputtering, can be a very good alternative high resistance transparent (HRT) layer for CdS/CdTe thin film solar cells [1] (chapter 6.2).
The application of a MZO layer on Indium Tin Oxide (ITO), substituting the standard ZnO layer has led to an increase of about 1 % in absolute efficiency compared to ZnO/ITO-contacted devices and of more than 2 % in absolute efficiency compared to single ITO contacted cells [1].
This can be explained by the fact that MZO results in higher transparency not only compared to CdS but even to ZnO, and, more important, it gives a better band alignment with CdS [2, 3]: MZO band gap can be tuned changing the substrate temperature during the deposition, and by doing so controlling the Mg content. This results in an increase in efficiency, in particular in terms of short-circuit current density as well as fill factor [1, 4].
In this sub-chapter, I analyze CdTe devices where the CdS layer is removed and substituted by MZO in order to increase the light absorbed by the CdTe and increase device efficiency. A similar approach has been presented by Colorado State University but for high substrate temperature CdTe [5, 6].
In the first step the MZO layer optimized for CdS/CdTe junction was applied to the CdS-free device, however this did not provide a good p/n junction; the cells do not exceed 6.5 % of efficiency, in particular open circuit voltage resulted in values below 670 mV. In this section I present a study for the preparation of MZO layer optimized to engineer an improved MZO-CdTe junction; a MZO layer was grown with different deposition parameters in the RF sputtering chamber such as oxygen content, chamber pressure and substrate temperature. Efficiencies above 12 % have been obtained, with remarkable open circuit voltage and superior values of current density.
The MZO layer has been characterized by X-ray diffraction, transmittance measurements, and its morphology has been studied by atomic force microscopy, whereas the finished samples have been characterized by current-voltage and external quantum efficiency measurements.

6.3.1 Experimental procedure

Images of the MZO morphology by Atomic Force Microscopy (AFM) were provided with a NT-MDT Solver Pro in semi-contact mode and NTMDT nsg-01 golden silicon tips. Current-voltage characteristics (JV) were obtained by using a Keithley SourceMeter 2420 at room temperature and 1000W/m^2 irradiance. The crystalline structure was analyzed with a Thermo ARL X'TRA powder diffractometer (in Bragg-Brentano geometry, equipped with a Cu-anode X-ray source (Kα, λ=1.5418 Å) and a Peltier Si (Li) cooled solid state detector). The transmission measurements have been obtained by a Unicam spectrometer Type UV2-100 in UV-visible range. The external quantum efficiency (EQE) was obtained at Department of Information Engineering, University of Padova, using a commercial LOANA solar cell analysis system. The EQE is calibrated with a silicon reference sample with known EQE using an incident spotlight of 1 mm x 2 mm area.

In our laboratory CdTe devices on superstrate configuration are prepared at temperatures not exceeding 450 °C. On a fluorine doped tin oxide (FTO) by Pilkington (TEC10), we deposit MZO by RF-sputtering with a 3 in. diameter target (MZO target contains 11 % MgO and 89 % ZnO Wt %, and it is 99.95% pure), in an argon and oxygen atmosphere, with a sputtering power density of 2.2 Wcm^{-2}. After that an annealing in air at 450°C is performed in order to favor the recrystallization of the film. Then we deposit about 7 μm of CdTe by vacuum evaporation with a substrate temperature of 340 °C. CdTe is treated by depositing a saturated solution of $CdCl_2$ in methanol and by annealing the stacks at 400 °C. The back contact is made by evaporation of 2 nm thick copper layer and 30 nm thick gold layer at room temperature after etching in bromine-methanol solution (15.5 g of Br_2 per liter of methanol). After back contact deposition, annealing of the finished devices at 200°C in air is necessary in order to deliver high efficiencies.

6.3.2 MZO layer fabrication

In order to optimize the MZO layer to engineer the MZO/CdTe junction, hundreds of samples have been fabricated with different deposition parameters; by varying them the composition of the MZO layer changes too.
From the transmission measurements of the MZO film, we can estimate the band gap of the material through the Tauc plot. For example, for an MZO deposited at 300°C, in a 50% O_2 on (Ar + O_2) atmosphere, with a chamber pressure of 3.6 Pascal, the estimated band gap is 3.72 eV (see the linear fit in figure 6.3.1).

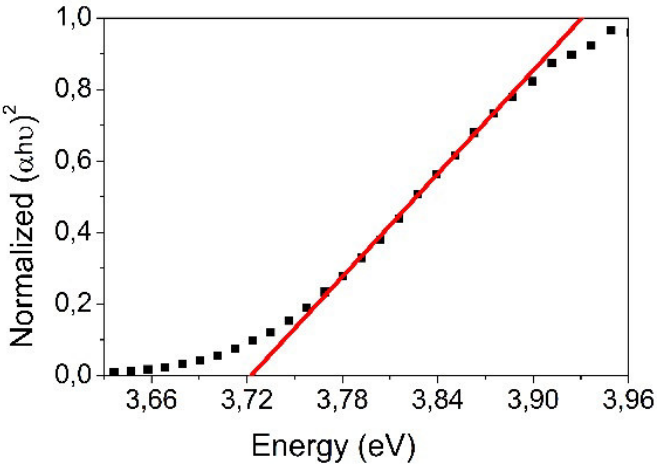

Figure 6.3.1: Tauc Plot based on the transmission measurements of a MZO layer deposited at 300°C, in a 50% O_2 on (Ar + O_2) atmosphere, with a chamber pressure of 3.6 Pascal.

Moreover it has been reported that in the range $0 < x < 0.46$ of the $Zn_{1-x}Mg_xO$ layer, the band gap of films widened linearly with the increase of the Mg content, and consequently the band gap range from the 3.24 eV of ZnO to 4.20 eV when $x = 0.46$ [7]. Referring to this linear relation, the MZO with a 3.72 eV wide band gap (in fig. 6.3.1) would have a Mg content of $x = 0.23$.
It has been previously reported that the Mg concentration can be influenced by the deposition temperature [1]. In table 6.3-I we compare MZO layers on soda lime glass fabricated with

different oxygen percentage and different substrate temperatures. The first two rows show samples with similar oxygen content but with different substrate temperatures, they have a very similar band gap and amount of Mg. When oxygen content is triplicated, as shown in the third row, the band-gap drops. In table 6.3-II MZO layers deposited on FTO/glass stacks with different substrate temperatures and oxygen content are compared, band gap value stays stable at around 3.7 eV irrespective of the deposition parameters, but if the vacuum pressure is increased of one order of magnitude the band gap drops of 0.1 eV. So by keeping the 50% of O_2 in chamber, but increasing the total chamber pressure (thus raising the O_2 pressure from 1.8 Pa to 25 Pa) the band gap further reduces from 3.72 eV to 3.63 eV.
A very large amount of solar cells have been fabricated with differently deposited MZO coated FTO/glass and devices fabricated with MZO deposited in O_2-poor atmosphere deliver lower efficiency, at least for low substrate temperature CdTe deposited in our lab.

Table 6.3-I: Deposition parameters and their respective band gap and Mg content of MZO samples deposited on glass substrates.

O_2 (%)	Chamber pressure (Pa)	Temperature (°C)	Band Gap (eV)	Mg content x
1.7	0.75	100	3.97	0.33
1.2	1.1	200	4.03	0.36
4.7	0.83	RT	3.77	0.25

Table 6.3-II: Deposition parameters and their respective band gap and Mg content of MZO samples deposited on FTO coated glass substrates.

name	O_2 (%)	Chamber pressure (Pa)	Temperature (°C)	Band Gap (eV)	Mg content x
	33.3	1.2	RT	3.78	0.25
MZO A	50	3.6	300	3.72	0.23
MZO B	50	50.0	300	3.63	0.18

6.3.3 Devices performance and characterization

Our best performing devices were fabricated with MZO layers with the narrower band gaps (see MZO A & MZO B in table 6.3-II).
The MZO/CdTe junction solar cells reach efficiencies up to 12.9 % (see left side in fig. 6.3.2 and table 6.3-III-first row). In this case, a 65 nm thick MZO layer has been deposited with a total chamber pressure of 3.6 Pascal in a 50% Ar, 50% O_2 atmosphere, and a substrate temperature of 300°C. This type of layer has been called MZO A and its band gap has been estimated to be 3.72 eV. After the deposition the FTO/MZO stack was annealed in air at 450°C. The JV characteristics show very high Voc and Jsc, with respective average values of (886 ± 8) mV and (26.8 ± 0.4) mA/cm^2, but low fill factors; statistically with this specific MZO A we obtain efficiency of (12.5 ± 0.4) %. Maintaining the same parameters and increasing the chamber pressure to 50 Pascal (MZO B: band gap of 3.63 eV), fill factor improves up to 57.1%, however the Voc decreases to around 760 mV, bringing to efficiency below 12 % (see right side in figure 6.3.2 and table 6.3-III-third row).

Thus as the MZO band gap becomes narrower (closer to that of ZnO), the Voc drops. In fact with a ZnO/CdTe junction, where the ZnO band gap is 3.24 eV, we obtained samples with an average Voc of (537 ± 16) mV, a FF of (47 ± 1) % and an efficiency of (5.9 ± 0.2) % (see table 6.3-III fifth row).

Table 6.3-III: Parameters of the best performing MZO/CdTe samples (cells shown in figure 6.3.2), and average values of the parameters of the samples made with two different MZO (MZO A & MZO B), with ZnO and with CdS.

	Chamber pressure	MZO band gap	Voc (mV)	Jsc (mA/cm^2)	FF (%)	Eff (%)
Best efficiency (MZO A)	3.6 Pa	3.72 eV	888	26,9	53.9	12.9
Average efficiency (MZO A)	3.6 Pa	3.72 eV	886 ± 8	26.8 ± 0.4	53 ± 1	12.5 ± 0.4
Best efficiency (MZO B)	50 Pa	3.63 eV	761	27.6	57.1	12.0
Average efficiency (MZO B)	50 Pa	3.63 eV	726 ± 30	26.4 ± 1.1	55 ± 2	10.6 ± 1.2
Average efficiency	ITO/ZnO/CdTe cell (no MZO)		537 ± 16	23.5 ± 0.6	47 ± 1	5.9 ± 0.2
Efficiency	ITO/ZnO/CdS/CdTe cell (EQE fig. 6.3.3)		852	25.4	72	15.6

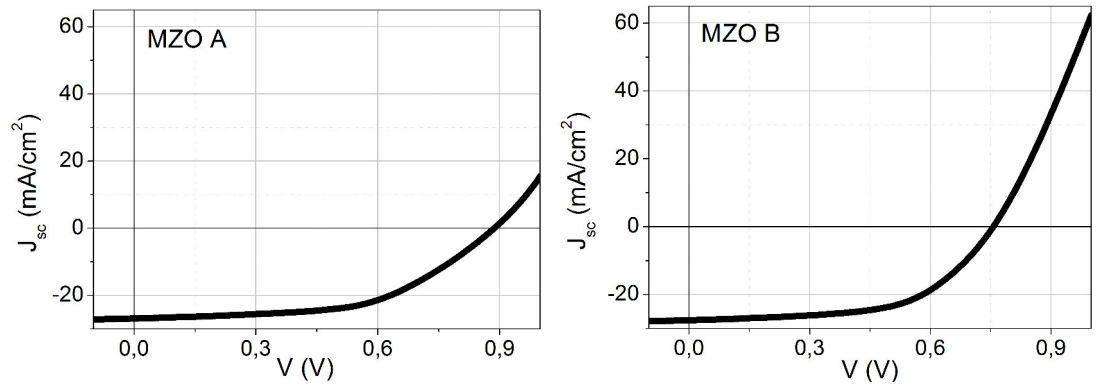

Figure 6.3.2: J-V characteristics of the best performing MZO/CdTe samples made with MZO A (left) and with MZO B (right). The efficiency parameters are presented in table 6.3-III.

In order to verify if the lack of the CdS window layer has led to an increase of the light absorbed by the CdTe, external quantum efficiency measurements have been performed. In figure 6.3.3 the EQE response of cells with different window layers is compared: black line refers to a 65 nm thick MZO layer (MZO A), while red line refers to a 150 nm thick CdS

layer (whose efficiency parameters are reported in table 6.3-III). With MZO as window layer (both MZO A and MZO B, not shown here, give the same result) a significant improvement in the short-wavelength region (330-550 nm) is achieved. On the other hand, we can observe a lower response in the 550-830 nm range. In the long-wavelength region, at wavelengths near the CdTe band-gap range, the MZO/CdTe curve (in black) is net separated from the curve of the standard CdS/CdTe cell. The formation of a CdS_xTe_{1-x} layer [8] allows absorption of photons with slightly less energy. This is not the case of the MZO/CdTe devices, where an abrupt interface is formed, as shown by Munshi et al. [6]: without an intermixed layer, which reduces the lattice mismatch, the formation of lattice defects is enhanced. These defects may be the cause of carrier recombination at the interface and of the FF reduction.
Another additional cause for the fill factor reduction could possibly also come from an insufficient doping of MZO [9], which results in a weaker driving electric field, bringing to lower carrier collection as suggested by the lower response of the EQE as mentioned above.
XRD patterns have been measured on the surface of the $CdCl_2$-treated CdTe, in order to calculate the lattice parameter of CdTe deposited on MZO A, through the Nelson Taylor plot method [10, 11].
We calculated a lattice parameter of (6.495 ± 0.003) Angstrom. This value is quite high if compared with the lattice parameter of the treated CdTe layer deposited on 30 nm thick CdS, which is (6.488 ± 0.001) Angstrom.
It has been already calculated that the lattice parameter of CdTe deposited on CdS decreases after the $CdCl_2$ treatment [12]. This is because during the treatment, the diffusion of Te and S in the CdTe/CdS interface leads to the formation of a CdS_xTe_{1-x} layer, thus the interfacial stress caused by the lattice mismatch between CdTe and CdS is reduced. Clearly this effect is not present with the MZO/CdTe abrupt interface, where it is also expected a larger lattice mismatch with CdTe relative to CdS [13].
The higher lattice parameter is an evidence of the compressive stress of CdTe deposited on MZO in the plane of film growth.

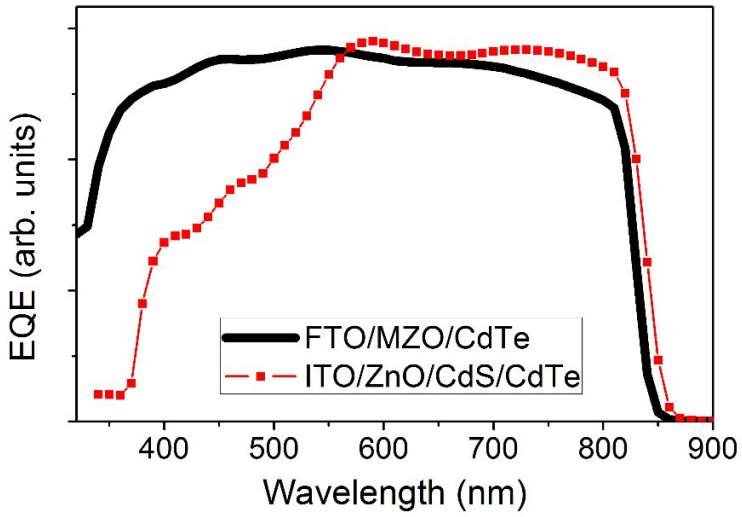

Figure 6.3.3: comparison of EQE response of devices with CdS/CdTe and MZO/CdTe junction.

6.3.4 MZO layer characterization

Further characterizations have been performed on the MZO layer with which we fabricated the best performing devices (MZO A).
The crystal structure of a 500 nm thick MZO A layer, deposited on FTO, has been investigated by XRD. Since after MZO deposition an annealing in air at 450°C is used to favour the recrystallization, a comparison between the XRD patterns of this layer before and after the annealing in air at 450°C is shown in figure 6.3.4.
In both cases the (002) peak from the crystallographic data of the hexagonal structure of ZnO is present, at this composition ratio (that is for $x < 0.58$ in $Mg_xZn_{1-x}O$), the basic structure MZO is the same of ZnO, thus hexagonal [7]. For the annealed case also the (101) ZnO peak is visible.
The other peaks are associated with the underlying FTO film, moreover, no Bragg reflections associated with MgO where found. In fact the (200) and (220) peaks indexed from the crystallographic data of the cubic structure of MgO are not present: the peak at about 62° (that would correspond to the (220) MgO peak) is actually associated with FTO.
The main difference between the spectra is that the annealed layer shows higher ZnO peaks; confirming a larger crystallization of this film.

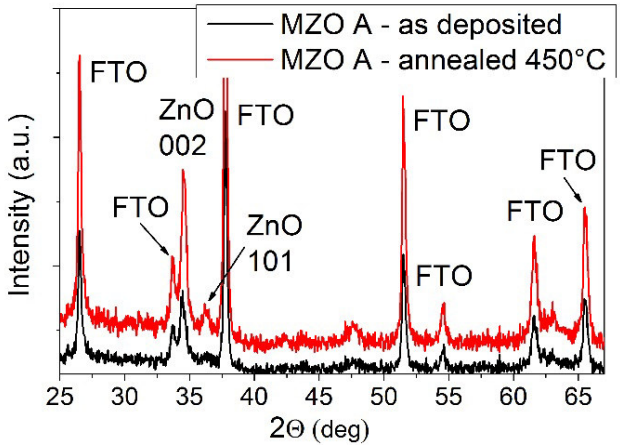

Figure 6.3.4: XRD patterns of MZO A layer deposited on FTO: as deposited (black line-below) and after the annealing in air at 450°C (red line-above).

Moreover, a morphology study of the surface of MZO, performed through atomic force microscopy (AFM), shows that the annealing leads to a grain rearrangement.
AFM images of the as deposited and annealed in air at 450 °C MZO A type layer, with which we obtained the best performing devices, are shown in fig. 6.3.5. A change of morphology is visible: before the annealing process (fig. A) the agglomerates of grains are maximum 60 nm wide, after (fig. B) they are up to 120 nm wide.

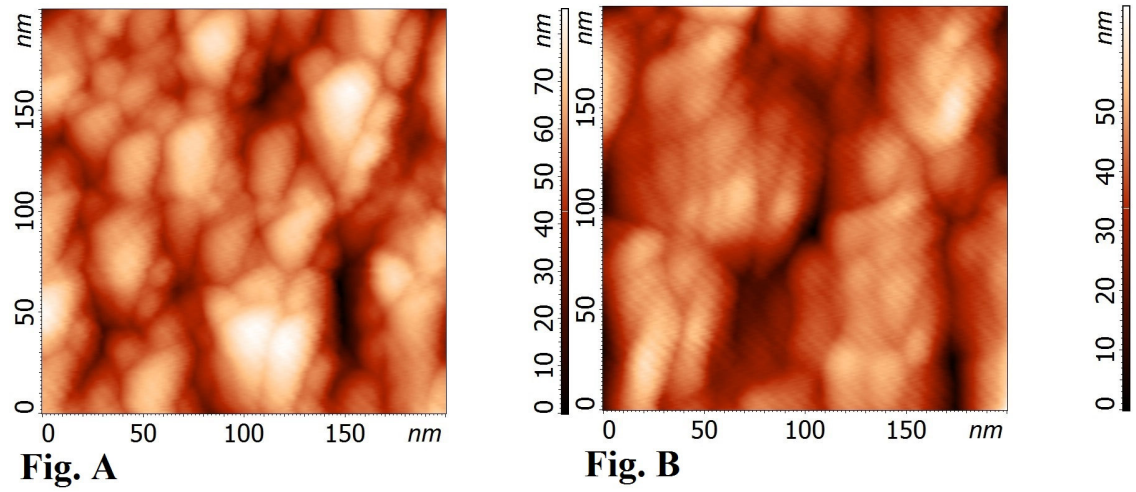

Figure 6.3.5: AFM images of MZO layer as deposited (A, on the left) and after a 450°C annealing in air (B, on the right).

6.3.5 Conclusions

We have fabricated low temperature CdTe solar cells in superstrate configuration by totally removing CdS, and by using MZO as buffer layer. Good efficiencies close to 13 % have been obtained, with Voc above 885 mV and short-circuit current of 27.0 mA/cm^2, but low fill factor. The EQE response confirms a significant absorption improvement in short-wavelength region (330-550 nm), well as a slightly lower collection of photoelectrons in the 550-830 nm range compared to the sample with CdS, suggesting a lower quality of the MZO/CdTe junction. This could be caused by the presence of a large amount of defects due to the reticular mismatch and possibly by an insufficient doping of MZO.
We have obtained the best performances using a $Mg_{0,23}Zn_{0,77}O$ with a band gap of 3.72 eV. The band gap of MZO films range between 3.63 eV and 4.03 eV. This variation is influenced by the O_2 content in the RF-sputtering chamber: with the 1-2 % of O_2 in chamber, MZO films show a band gap around 4.0 eV, whereas increasing the percentage from 4.7 up to 50, the MZO band gap drops around 3.72 – 3.78 eV. Moreover, with the 50% of O_2, but increasing the chamber pressure to 50.0 Pa, consequently increasing the O_2 contents, the band gap drops to 3.63 eV. Thus, the magnesium contents in the MZO film is also influenced by the amount of O_2 present in the chamber.

6.3.6 References

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Study of the alternative $MgCl_2$ activation treatment

CdTe-based solar cell has demonstrated to be so far one of the best thin film photovoltaic technologies, reaching laboratory conversion efficiencies of more than 22% [1]. One of the key factors for the success of these devices is the so-called "activation" treatment, which typically consists in depositing a $CdCl_2$ film on the CdTe absorber layer and in a subsequent annealing in air or nitrogen atmosphere [2]. Nevertheless, $CdCl_2$ is a highly toxic and carcinogenic chemical agent and water-soluble compound and for this reason its usage and disposal need strong safety procedures. For this reason, alternative activation treatments have been experimented and among them $MgCl_2$ treatment is one of the most successful option, reaching conversion efficiencies of about 15% [3]. $MgCl_2$ is a non-toxic chemical and its usage does not need special and strict restrictions. However so far, at laboratory scale, solar cells treated with $MgCl_2$ have not reached the efficiencies of the world record $CdCl_2$-treated ones and for this reason $CdCl_2$ is still preferred. In order to better understand the $MgCl_2$ treatment mechanism and the reasons for its lower efficiency, two sets of CdTe-based solar cells have been fabricated with our usual process [4]. One set has been activated with the standard $CdCl_2$ treatment, while the other one with $MgCl_2$ treatment. The solar cells have been electrically characterized by means of current-voltage (J-V), capacitance-voltage (CV), drive level capacitance profiling (DLCP) and admittance spectroscopy (AS) techniques and the results for the two sets have been compared in order to address the differences in terms of electrical properties.

7.1.1 Experimental procedure

CdTe solar cells have been fabricated in superstrate configuration. The front contact is deposited on top of a 3 × 3 cm^2, 4 mm thick, soda lime glass and it is produced as ITO/ZnO bi-layer stack. A 400 nm thick indium tin oxide (ITO) film is deposited by a customized RF reactive magnetron sputtering system, starting from a 90% In_2O_3:10 % SnO_2 target. The film is deposited in a reactive atmosphere of Ar + 2–3 % O_2 at a substrate temperature of 400 °C. The front contact is completed by covering the ITO layer with a 100 nm thick i-ZnO film, with the same sputtering machine, starting from a metallic Zn target, in a reactive atmosphere of Ar + 10–20 % O2 at a substrate temperature of 400 °C. The front contact is then covered with a CdS layer, which is deposited by high vacuum thermal evaporation. Also in this case the deposition system used is a customized one. Pieces of sintered CdS are put into a tungsten crucible and heated up, in order to obtain a vapor flux corresponding to a deposition rate of about 1 nm per second. The CdS film is deposited at a substrate temperature of 100 °C, with a thickness of 200– 300 nm. The p-n junction is completed depositing the CdTe film in the same deposition machine, again by vacuum evaporation. A graphite crucible is filled with CdTe crystals and heated up, obtaining a vapor flux rate of about 20 nm per second. In these conditions CdTe deposition takes place at a substrate temperature of 340 °C, until a film thickness of about 5–6 μm is reached. As already mentioned, two different activation

treatments are applied after CdTe deposition and both consist in dissolving the activating agent ($CdCl_2$ or $MgCl_2$) in methanol, applying a specific amount of the resulting solution on the CdTe surface and annealing the stacks in air. The solutions have been prepared with different concentration levels and applied in form of drops, deposited onto the sample surface, in microliter volumes. The annealing in air of the sample is performed at temperatures ranging between 365 and 410 °C, for about 30 min. After the application of the activation treatment it is possible that some solution residuals remain on the CdTe surface, altering the electrical contact between the CdTe and the final back contact. In order to prevent this, an etching with Br-methanol solution is performed, which also promotes the formation of a p+ Te rich layer on the CdTe surface. The back contact is produced by depositing a 2 nm thick Cu and a 50 nm thick Au films by vacuum evaporation, with the substrate kept at room temperature, using a customized high vacuum thermal evaporator starting from pure metallic shots. In order to allow Cu to better interact with the Te rich surface, the device is annealed in air at 190 °C for 20 min.

7.1.2 Results and discussion

To understand the effect of the $MgCl_2$ treatment with respect to the $CdCl_2$ one, we decided to compare cells made with the same process but with different activation conditions. In the case of $CdCl_2$, samples have been prepared using $CdCl_2$ solution of different concentrations, namely 20 %, 30 % and 50 % of saturation and different volumes, from 60 to 300 µl.

Table 7-I: Photovoltaic parameters of solar cells treated with different $CdCl_2$ solutions.

$CdCl_2$-sample treatment	Treatment temperature	J_{SC} (mA)	V_{OC} (mV)	FF (%)	η (%)
20 % $CdCl_2$ 150 µl	410 °C	17.3	803	58.3	8.1
30 % $CdCl_2$ 300 µl	390 °C	23.7	831	66.1	13.0
50 % $CdCl_2$ 150 µl	380 °C	25.6	859	70.9	15.6

In table 7-I the main results obtained with this process are summarized. The J-V characterization has been performed using a self-modified solar simulator, equipped with a specific Osram Decostar 51 Eco Superstar (35 W, 550 lm) halogen lamp, calibrated with a Si solar cell. Data have been recorded by using a Keithley source meter 2420. Best results have been found in using 150 µl of a 50 % saturated $CdCl_2$ solution, which have been set as our reference values for the $CdCl_2$ sample. The reference sample exhibited an efficiency of 15.6 % (Voc = 859 mV, Jsc = 25.6 mA/cm^2, FF = 71 %). A similar approach has been followed also in the case of $MgCl_2$ and the main results for this second process are shown in table 7-II.

Table 7-II: Photovoltaic parameters of solar cells treated with different $MgCl_2$ solutions.

$MgCl_2$-sample treatment	Treatment temperature	J_{SC} (mA)	V_{OC} (mV)	FF (%)	η (%)
20 % $MgCl_2$ 100 µl	380 °C	23.7	789	66.1	12.4
20 % $MgCl_2$ 200 µl	380 °C	23.4	761	59.8	10.6
50 % $MgCl_2$ 60 µl	380 °C	23.7	838	65.5	13.0
50 % $MgCl_2$ 200 µl	395 °C	23.2	782	62.7	11.4

In this case, a champion cell with 14.3 % efficiency (Voc = 852 mV, Jsc = 23.6 mA/cm^2, FF = 71 %) has been obtained by treating the sample with 140 µl of the 20 % $MgCl_2$ saturated solution. Even if solar cells fabricated with the two processes have similar conversion efficiencies, the ones treated with $CdCl_2$ have reached higher photovoltaic parameters.

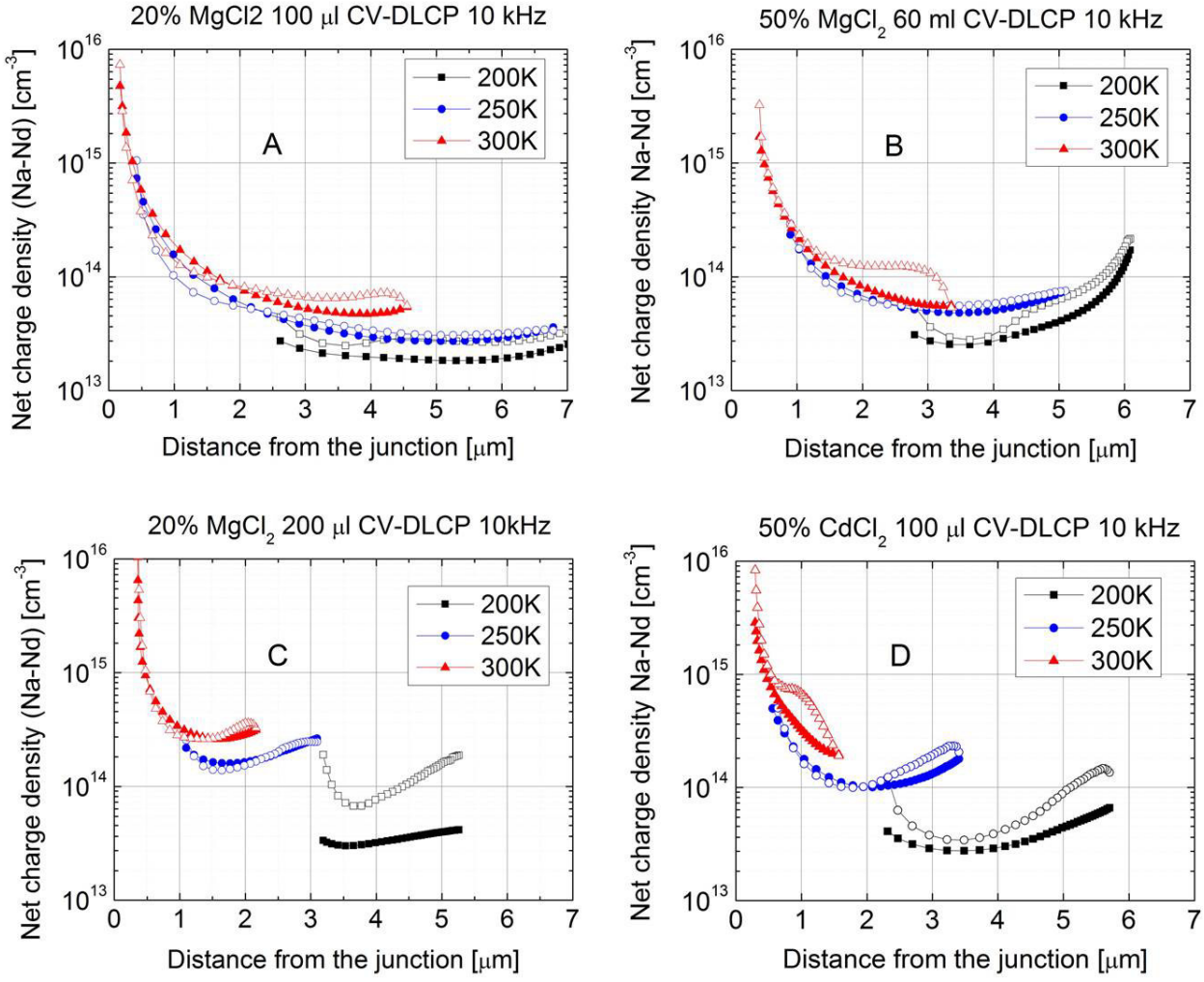

Figure 7.1: Comparison between CV (open dots)/DLCP (full dots) spectra of samples treated with different concentration and/or amount of a), b) and c) $MgCl_2$ and d) $CdCl_2$ solutions at different temperatures.

Samples have been characterized also by CV and DLCP measurements, in order to obtain a correlation between the treatment parameters and their effect on the electrical properties of the devices. These measurements have been performed in a Janis cryostat with an HP 4284 A LCR meter, at a pressure of 10^{-4} Pa and with a Lakeshore 325 system temperature controller. Measurements have been done at temperatures ranging from 200 K to 300 K and at frequency values of 10 kHz, 100 kHz and 1 MHz for studying the defect response evolution. In figure 7.1 a comparison of representative CV/DLCP spectra are shown. Data were collected at a frequency of 10 kHz, with samples respectively treated with (A) 100 and (C) 200 µl of the 20 % $MgCl_2$ solution and (B) 60 µl of the 50 % $MgCl_2$ one. In fig.7.1 D the data of the reference $CdCl_2$ treated sample are also shown. When 200 µl of 20 % $MgCl_2$ solutions and even more concentrated
ones are applied, the CdTe charge density is higher being over 10^{14} cm^{-3} and it extends for more than 2 µm from the junction. As the amount of the treatment solution used increases, also the carrier
charge density increases. In fact Cl-based treatment promotes the intermixing between CdS and CdTe active layers at the junction and enables a recrystallization of the CdTe absorber layer. All these phenomena result in a reduction of the lattice mismatch at the p-n junction and as a consequence also in a decrease in the interface defect density, which are carrier traps and act as a barrier for the current transport. Nevertheless, by considering the photovoltaic parameters of table 7-II it can be noticed that for $MgCl_2$ treatments stronger than 60 µl of 50 % concentrated solution, samples start to have lower open circuit voltage (Voc) and then lower efficiencies. This behavior can be related to a different defect concentration inside the active materials, which can be explained by the difference in their CV and DLCP spectra (fig. 7.1-A, B). Since DLCP is a more selective technique for shallow defects, while by CV it is possible to obtain information about the kinetics of carrier transport through both shallow and deep defects, from the comparison of their spectra and more precisely from their difference it can be estimated a qualitative concentration of deep defects into the material studied [5]. With low amount of solution (100 µl, 20 % concentration: fig. 7.1-A), considering the room temperature profiles, the device shows a low carrier concentration (in the 10^{13} cm^{-3} range) with an evident separation between DLCP and CV. On the other hand, with 200 µl of the 20 % concentration solution (fig.7.1-C) the charge density increases up to the 1×10^{14} cm^{-3} range but DLCP and CV are superposed (at 300 K), suggesting that over a certain $MgCl_2$ quantity, the deep defects are compensated. This is also supported by the fact that for samples with $MgCl_2$ 20 % concentrated solution the CV lines are below DLCP even at 300 K, which can be explained by a compensation of the deep defects.
Also, at lower temperatures the difference between CV and DLCP increases, this can be explained again by the fact that compensating defects are not activated. The CV/DLCP graphs of the $MgCl_2$ treatment that mostly resemble the $CdCl_2$ treatment ones are those corresponding to the solar cells
with the best efficiencies, which have been treated with 60 µl of 50 % concentrated $MgCl_2$ solution (fig. 7.1-B). They show a charge density in the 1×10^{14} cm^{-3} range and no compensation effect. Despite the similar shape of CV/DLCP spectra, at 300 K $CdCl_2$ treated devices exhibit a charge density larger than any of the best samples processed with $MgCl_2$ treatment. These samples have CV/DLCP curves concentrated in the first 3 µm of CdTe layer, closer to the junction and this can be explained by a higher doping that reduces the depletion region. At the same time, the $CdCl_2$ treated solar cells show a larger quantity of deep defects.

Admittance spectroscopy has been performed using the same equipment for DLCP and the characterization has been obtained applying to the samples DC biases, of −0.5 V, 0 V and +0.5 V, superposing another signal with a frequency sweeping from 300 Hz to 1MHz and at temperatures
between 90 K and 320 K. In table 7-III, defects calculated from admittance spectroscopy of differently $MgCl_2$ treated devices are shown.

Table 7-III: Energy and cross-sections of defects calculated by admittance spectroscopy.

100 µl 20 %			
E_a [meV]	Err [meV]	S_a [cm^{-2}]	Possible identification
83	1	$3.0 * 10^{-19}$	Impurities from the front contact/glass [6]
110	1	$8.7 * 10^{-17}$	A center V_{Cd}-Cl_{Te} [7]
129	2	$1.9 * 10^{-16}$	A center V_{Cd}-Cl_{Te} [7] or V_{Cd} V_{Te} [8]
143	1	$7.2 * 10^{-16}$	A center V_{Cd}-Cl_{Te} [7] or V_{Cd} V_{Te} [8]
153	2	$2.8 * 10^{-15}$	A center V_{Cd}-Cl_{Te} [7] or V_{Cd} V_{Te} [8]
228	4	$3.9 * 10^{-17}$	Cu^{2+} [8]
344	4	$2.3 * 10^{-14}$	Not identified
358	1	$2.2 * 10^{-14}$	Not identified
403	5	$7.8 * 10^{-13}$	Cl^{+}_{Te} [8]
425	1	$1.9 * 10^{-13}$	Cl^{+}_{Te} [8]
549	2	$1.9 * 10^{-11}$	Te^{2-} [8]

60 µl 50 %			
E_a [meV]	Err [meV]	S_a [cm^{-2}]	Possible identification
117	3	$3.1 * 10^{-16}$	A center V_{Cd}-Cl_{Te} [7]
128	2	$2.8 * 10^{-15}$	V_{Cd} V_{Te} [8]
150	1	$3.5 * 10^{-14}$	V_{Cd} V_{Te} [8]
295	5	$1.6 * 10^{-16}$	Te_{Cd} / Cu_{Cd} [9] or V_{Cd} V_{Te} [8]
322	4	$2.9 * 10^{-16}$	Te_{Cd} / Cu_{Cd} [9] or V_{Cd} V_{Te} [8]
401	6	$2.1 * 10^{-14}$	Cl^{+}_{Te} [8]
411	5	$1.6 * 10^{-12}$	Cu^{-}_{Cd} or Cl^{+}_{Te} [8]
416	12	$1.4 * 10^{-13}$	Cu^{-}_{Cd} or Cl^{+}_{Te} [8]
424	13	$2.2 * 10^{-12}$	Cl^{+}_{Te} [8]
526	6	$2.1 * 10^{-11}$	Te^{2-} [8]
537	7	$3.1 * 10^{-11}$	Te^{2-} [8]
615	15	$3.2 * 10^{-9}$	Cl^{+}_{Te} [8]

In case of samples treated with 100 µl of a 20 % concentrated solution (table 7-III), a low energy defect at about 83 meV is detected, which could be attributed to impurities from the front contact [6]. From 110 meV up to 160 meV the typical acceptors, such as A centers (V_{Cd}-Cl_{Te}) [7] and/or Cd/Te vacancies [8] are detected. These defects have been observed also in samples treated with 200 µl of 20 % and 50 % concentrated solutions. On the other hand, only these latest samples exhibited defects between 280 and 300 meV. Castaldini et al. [9] identified these defects as Te_{Cd} interstitials and they might be partly responsible for the lower efficiency of the samples treated with larger amount of $MgCl_2$ solution. Two deep defects, at 344 and 358 meV, have been measured but not identified; only the best working devices did not exhibit these defects.
These defects could be connected with Mg, since no similar defects have been detected previously for $CdCl_2$ treated devices. From table 7-III, it can be finally noticed that for the best devices (processed with lower amount of higher concentrated $MgCl_2$ solution) the detected defects are very similar to those previously observed in the $CdCl_2$ case: mid gap defects, attributed to $MgCl_2$ treatment, as well as Cu-related ones. For an optimal quantity of $MgCl_2$ solution treatment, devices behave more likely to $CdCl_2$ ones because both are characterized by the same nature of defects, but probably a difference in their concentrations can justify the lower photovoltaic parameters of $MgCl_2$ solar cells.

7.1.3 Conclusions

$MgCl_2$ has demonstrated to be a good alternative to the conventional $CdCl_2$. Solar cells with efficiencies exceeding 14 % can be obtained by simply changing the treatment agent from $CdCl_2$ to $MgCl_2$. However devices produced with $CdCl_2$ still exhibit a slightly higher efficiency and this could be related to the lower charge density and to a different structure of defects for the $MgCl_2$ treated samples. Treatments with larger quantity of $MgCl_2$, exhibited

an increase in charge density but at the same time also increased deep defect compensation, resulting in lower performances.
Moreover two unidentified defects have been detected in any $MgCl_2$ treated samples except for the ones with the highest performance. These defects have never been observed in any of our $CdCl_2$ samples and for this reason they have been generally attributed to the $MgCl_2$ treatment.

7.1.4 References

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8
Study of alternative back contact

8.1 Introduction of MoOx at the back contact

CdTe thin film solar cells are the most successful thin film photovoltaic devices in terms of production yield, as attested by the remarkable market performance. Nevertheless, the device has also shown to be competitive in terms of efficiency as attested by the latest results from First Solar, where a record efficiency of 22.1% has been obtained [1]. One of the main issues for CdTe devices stability is the nature of the back contact. Because of the CdTe high electron affinity the insertion of copper has demonstrated to deliver higher efficiency, but on the other side the copper diffuses into the CdTe bulk degrading the cell. Moreover recent works have shown that copper is a crucial element for the CdTe doping and consequently for high conversion efficiency [2]. To analyze the effect of copper doping it is necessary to remove it at the back contact in order to avoid uncontrolled copper diffusion in the absorber. At the same time it is important to apply a metal with a suitable electron affinity to form a good ohmic contact with CdTe. Recently, MoO_3 has been successfully applied for back contact performing good efficiencies on high temperature deposited CdTe by close space sublimation [3]. Due to its high work function of about 6.8 eV, MoOx is one of the few semiconductors able to form an ohmic contact with p-type CdTe. In the work presented in this sub-chapter, I try to optimize MoOx layer deposited by radio frequency sputtering in order to produce a performing back contact without application of copper. Then the devices have been prepared with different copper thicknesses in order to optimize its quantity to dope CdTe avoiding shunts. I present a study on the effect of MoOx buffer and copper doping on low substrate temperature vacuum evaporated CdTe. CdTe solar cells with different copper thicknesses are analyzed to understand the copper miscibility into the CdTe matrix so to find the right compromise between copper doping and copper shunting.

8.1.1 Experimental procedure

CdTe thin film solar cells were made in superstrate configuration by low-temperature fabrication process based on vacuum evaporation (VE). On an ITO/ZnO stack as front contact, 300 nm thick CdS thin film is deposited at 100 °C and then annealed at 450 °C in vacuum. Subsequently CdTe layer, with a thickness of 5 to 6 microns, is deposited in the same vacuum chamber and subsequently activated by $CdCl_2$ treatment applied by wet deposition and annealed in air at 380 °C. In our standard cells this treatment is followed by Br-MeOH etching in order to have a tellurium rich region, but in the case of these devices we only clean the surface of CdTe with distilled water. We usually deposit a 2 nm thick copper layer, which has the task of doping CdTe and making a good contact at the same time. In these cells, in order to analyze the doping effect, copper has been inserted prior the back contact deposition, with thicknesses in the range of 0.15 to 1 nm. The process is applied in a dedicated vacuum chamber

with a quartz crystal thickness monitor (Intellemetrics IL150). After deposition the stacks are annealed at 200°C for 30 minutes in vacuum to favor the diffusion of copper in CdTe. Back contact is made by reactive sputtering of molybdenum (target 99.95% pure) in argon/oxygen atmosphere for MoOx deposition, followed by sputtering of pure molybdenum or by vacuum evaporation of gold. MoOx deposition is carried on by Radio Frequency (RF) sputtering technique after reaching a vacuum of 10^{-6} mbar, with a power of 100 W and a chamber pressure of 5 * 10^{-3} mbar, and Mo with 220 W and 10^{-3} mbar. Substrate temperature is kept for both materials at room temperature (in order to avoid excessive diffusion of copper). Finally the samples are annealed in the furnace at 200°C for 30 minutes in air. The transmission measurements have been obtained by a Unicam spectrometer Type UV2-100 in UV-visible range. Raman spectra were collected with a Horiba Jobin-Yvon LabRam HR800 microprobe setup (in backscattering geometry) by using an exciting radiation at 632.8 nm (He-Ne laser). The current–voltage characteristics (J-V) were measured at room temperature by a Keithley 2420 Source Meter, using a calibrated halogen lamp with an irradiation of 1000 W/m^2.

8.1.2 results and discussion

We deposit MoOx by reactive radio frequency sputtering of molybdenum in argon/oxygen atmosphere at room temperature. Comparing MoOx and Mo thin films with similar thicknesses it results that the first one is transparent and shows high resistivity, while the second one is reflective in the visible region showing a good conductivity, roughly showing the positive results of reactive sputtering. Different MoOx thin film layers have been deposited on glass and their transparency has been measured with a UV/visible/IR spectrophotometer. As shown in figure 8.1.1, the transparency is very similar for both 20 and 50 % oxygen/(argon + oxygen) content in the sputtering system, suggesting a similar band gap. In fact, for both films we have calculated a bandgap of about 3.5 eV, in the same range identified by Simchi et al. for MoO_3 [4].

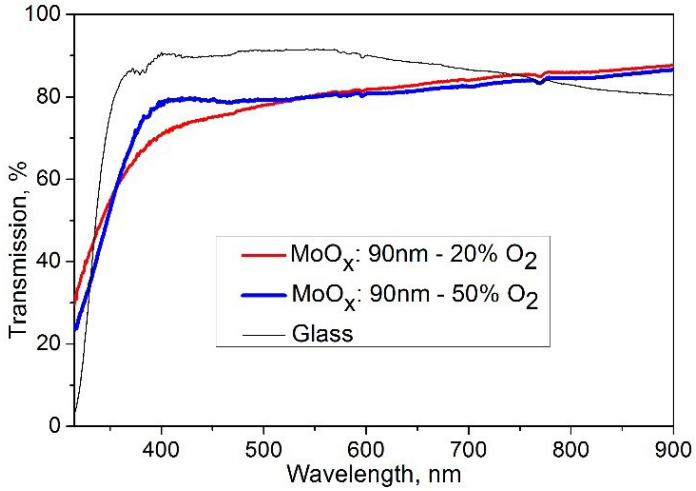

Figure 8.1.1: Transmission measurements of MoOx at different oxygen content.

However in the Raman analysis, different peaks have been detected, showing a slightly different structure of the layers. In the case of 20 % oxygen/(argon + oxygen) ratio, the Raman bands assigned to the terminal oxygen stretching at 995 cm^{-1}, triply connected bridge oxygen stretching mode at 666 cm^{-1} and the doubly connected bridge oxygen stretching at 821 cm^{-1} (see figure 8.1.2, top) are typical of MoO_3 layer. On the other hand, for the 50 % oxygen/(argon + oxygen) ratio, the observed peaks (at 777 cm^{-1}, at 852 cm^{-1} and at 950 cm^{-1}) are attributed to a layer of MoO_{x-3} [5]. During micro raman analysis with an incident laser power higher than 1.5 mW, the above mentioned peaks increase with time, showing a laser induced transformation from amorphous to crystalline structure. Also finished devices have been fabricated with 20 % and 50 % oxygen/(argon + oxygen) ratio. With excessive amount of oxygen in the sputtering chamber, the current and therefore also the efficiency is limited probably by a high back contact barrier. For this reason the CdTe cell fabrication process has been optimized by applying 20 %
$O_2/(Ar+O_2)$ deposited MoOx. Moreover, solar cells have been grown with different thickness of MoOx. With a 9 nm thick layer the current voltage characteristic begins to show a marked roll-over, for this reason our devices have been optimized with a 4-5 nm thick MoOx layer. The explanation can be attributed to the high resistivity of MoOx.

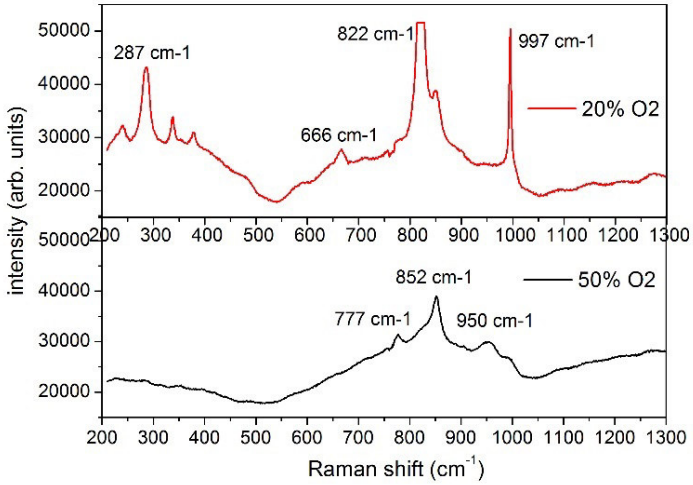

Figure 8.1.2: Raman plots of MoOx deposited by reactive sputtering, top with 20% O_2 over $(Ar+O_2)$ ratio, bottom with 50 % O_2 over $(Ar+O_2)$ ratio.

In figure 8.1.3 J-V characteristics of solar cells with different copper thicknesses are shown. The cells were prepared with our standard process and prior to the MoOx/Mo back contact, a very thin layer of copper was deposited by vacuum evaporation, and the stacks were annealed in air at 200 °C for 30 minutes for enhancing Cu diffusion into CdTe and doping it. First of all, different J-V behavior in the first quadrant of figure 8.1.3 is observed: roll over is inversely proportional to the Cu amount. This shows that copper is still acting as back contact when thickness is above 0.5 nm. Moreover, the main difference in performance is due to the current density, whereas open circuit voltage and fill factor exhibit similar values. This would suggest a different doping of the CdTe according to the copper thickness, however the samples have also different back contacts so definitive conclusions cannot be made.

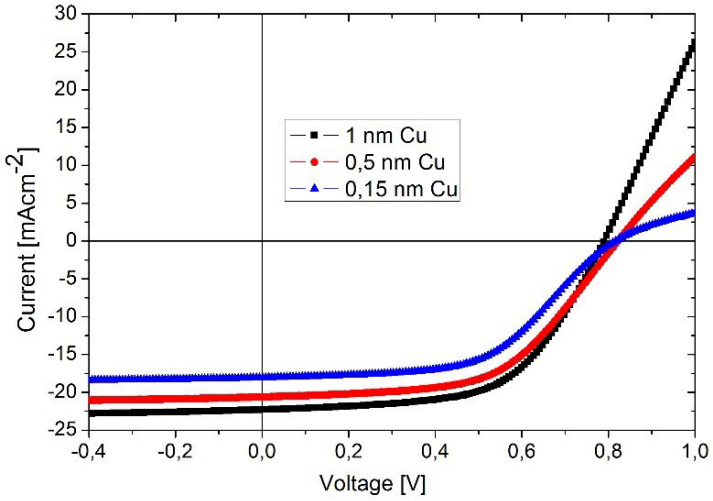

Figure 8.1.3: J-V of CdTe solar cells with MoOx/Mo back contact and different thickness of copper.

Table 8.1-I: Electrical parameters for cells with different copper content.

Copper content	Eff (%)	FF (%)	Jsc (mA/cm^2)	Voc (mV)
0.15 nm	7.9	53.6	18.0	817
0.5 nm	9.4	55.3	20.6	824
1.0 nm	10.3	58.0	22.3	796

To avoid that copper making contact in place of MoOx, the cells have been optimized by applying 0.15 nm thick Cu and subsequent annealing in vacuum at 200 °C for 30 minutes. Moreover in order to enhance Cu diffusion into CdTe we do not perform the Br-MeOH etching on the surface of CdTe: Rimmaudo et al. show how the copper reacts with Te forming CuTe and keeping Cu at the back contact [6]. Instead, the sample has been rinsed in water to remove surface residues from the $CdCl_2$ activation treatment. In order to reach good efficiencies, after the deposition of the back contact, a second annealing at 200 °C in air is needed. Comparing cells contacted with and without MoOx followed by Mo, there are no significant differences in efficiency: cells with MoOx show an improved current, but also with larger roll over. This could be explained supposing that MoOx is blocking the carriers, since the electron affinity of the MoOx made by sputtering could be too low [7]. It could also be that the Cu diffusion during the second annealing in air destroy MoOx layer. Moreover without copper the samples do not perform sufficient conversion efficiency.

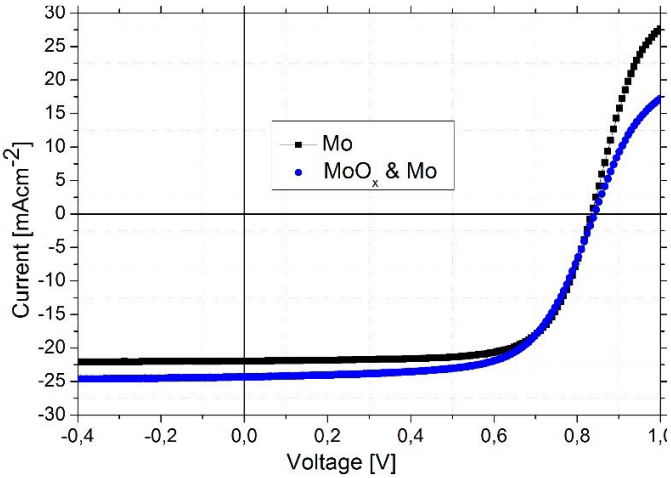

Figure 8.1.4: J-V of CdTe solar cells with MoOx/Mo and Mo back contact.

Table 8.1-II: Electrical parameters for cells with MoOx/Mo and Mo back contact.

contact	Eff (%)	FF (%)	Jsc (mA/cm^2)	Voc (mV)
MoOx & Mo	13.4	65.2	24.3	845
Mo	12.9	70.2	22.0	838

Back contacts with Au have been also made, the typical back contact in our laboratories are with 2 nm thick copper and 50 nm thick gold layer, instead in this work copper was reduced to 0.15 nm thick. Cells with and without MoOx between copper and gold have been compared. A first interesting point is that after the second annealing at 200 °C in air, performed on the completed device, the cells show low efficiencies, very different from our standard devices that after this annealing improve their efficiency up to 15 %. Probably with this annealing still the copper does not diffuse from gold into CdTe, suggesting that Cu is still at the contact working better without MoOx layer. After a third annealing at 300 °C in air the cells reach fairly good efficiency, but they show a very strong roll over meaning that Cu is diffused into CdTe, doping the absorbent layer, but also reducing performance of the back contact. We can see from the J-V curve, that in both cases after the second and the third annealing, the best contact is without MoOx: after the second copper reacts forming back contact and after the third probably because Cu diffuses in the bulk and also into the MoOx layer reducing the energy barrier.

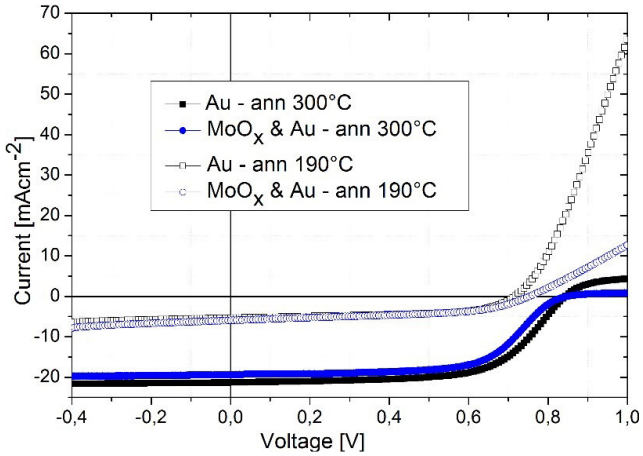

Figure 8.1.5**:** J-V of CdTe solar cells with MoOx/Au and Au back contact.

Table 8.1-III: Electrical parameters for cells with MoOx/Au and Au back contact.

Copper content	Eff (%)	FF (%)	Jsc (mA/cm^2)	Voc (mV)
MoOx/Au 190°C	2.3	49.9	6.0	761
Au 190°C	2.2	58.0	5.4	719
MoOx/Au 300°C	10.2	61.6	19.4	852
Au 300°C	11.4	63.5	21.3	845

In order to study the aging, cells contacted by MoOx/Mo and by Mo have been put for two weeks in accelerated stability test (AST) box under 1 sun illumination and at a controlled temperature of 80 °C. A set of cells has been aged in open circuit conditions (OCC) and a set in short circuit conditions (SCC) by applying a conductive wire between the front and the back contact [8]. We can see that the cells with MoOx layer aged in OCC suffer from a higher degradation; instead the performance reduction of cells without MoOx is almost independent on the applied bias. Usually our standard
cells have a very stronger degradation in OCC than in SCC, as in case of MoOx & Mo contact cells.
The fill factor decrease seems to have a greater impact on the degradation of the performance; this could be related to the back contact degradation. Probably the copper diffuses into CdTe, which now directly faces the MoOx or Mo layers. These devices deteriorate faster than our standard cells, because the copper is not blocked by the Br-MeOH etching (no CuTe compound is formed) and/or MoOx/Mo are less stable than Au. Current is not significantly affected by aging, but despite copper diffusion current density does not improve. In any case the temperature of 80 °C in the AST box is not enough to favor the solubility of copper in the CdTe bulk material.

Table 8.1-IV: Parameters normalized to initial ones in % for aged cells with MoOx/Mo and Mo back contact after 335 h.

Copper content		Eff (%)	FF (%)	Jsc (mA/cm^2)	Voc (mV)
MoOx/Mo	SCC	73	80	99	92
MoOx/Mo	OCC	55	65	97	88
Mo	SCC	75	80	100	93
Mo	OCC	74	81	99	92

8.1.3 Conclusions

We have deposited MoOx by reactive sputtering of molybdenum in argon/oxygen atmosphere with 20 % and 50 % O2/(Ar+O2) ratio: they show the same bandgap of about 3.5 eV, but with 50 % O2/(Ar+O2) ratio the efficiency is limited by high back contact barrier. 4-5 nm MoOx thick layer have been deposited because with thicker layers the J-V characteristics show a marked rollover. Comparing cells with MoOx/Mo and Mo contact we can see a small improvement in the current density and consequently an improvement of efficiency, but also an increased roll over which reduces the fill factor. However with this back contact the efficiency is very similar to the standard cells made in our labs but by using less than a tenth of copper thickness, so a greater amount of copper is not needed for doping CdTe. On the other hand these cells degrade faster probably due to a greater instability of the back contact. So degradation is not directly linked to the amount of copper content. Moreover we compared MoOx/Au with only gold back contact. These samples do not reach the efficiency of those mentioned above. MoOx deposited by reactive sputtering does not make a perfectly ohmic contact with low substrate temperature CdTe. Previous studies have shown that electron affinity is too low for sputtered MoOx [7].

8.1.4 References

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8.2 Study of a thin Cu layer

Despite various materials have been introduced at the back contact in order to enhance its ohmicity, such as ZnTe [1], Te [2,3] or MoO_x [4], Cu is present in all the most performing CdTe devices. The presence of copper has always been considered fundamental to attain higher efficiency devices. Generally copper is introduced at the back contact in order to reduce the Schottky barrier through the formation of Cu_xTe_{1-x} phases and the increase of the carrier concentration in the near CdTe region. In fact, Cu diffuses and produces a "p^+" layer at the near CdTe surface which allows carriers to tunnel though the barrier [5]. However, Cu is a fast diffuser in CdTe and an uncontrolled copper diffusion is widely considered the main cause of degradation of these devices. The doping and degradation mechanisms of Cu are still not well understood, and for this reason they are an important topic. The achievement of a high hole density by means of doping is one of the major challenges of CdTe solar cells research, as it is the way to improve the open circuit voltage and attain even higher efficiencies. Cu dopes CdTe through the formation of substitutional impurities Cu_{Cd}, but it also acts as a donor in interstitial positions, decreasing the hole density. Thus it has been theorized that an excessive Cu diffusion compensates the CdTe doping [6-8], decreasing the net charge density and thus leading to a performances decay. To overcome this problem many groups are focusing on the study of other p-type dopants such as P and As, which until now, however, have not led to better performances.
In this chapter, I have studied the influence of the thickness of the copper layer on the performances and on the degradation mechanisms of the devices. With different copper thicknesses, different approaches are needed to reach high efficiency; moreover the devices degrade with different mechanisms. In particular, superstrate configuration samples with a 0.1 nm thick copper layer have been fabricated and studied, as already done by Kranz et al. [6] for substrate configuration devices, in order to investigate how a minimum amount of intentionally added Cu affects the CdTe doping.
Samples with a lower Cu amount show a higher net charge density, suggesting a lower amount of compensating defects. On the other hand, these samples have lower efficiencies, mainly due to a strong roll over, symptom of a high back contact barrier. Surprisingly, they also show the inversion of the bias dependency during accelerated stress tests. In fact, they are more stable in open circuit aging condition, while generally, samples with intentionally added Cu are more stable in short circuit aging condition [9-12]. Thus in samples with a

lower Cu amount aged in short circuit condition another degradation mechanism predominates.

8.2.1 Experimental procedure

Current density-voltage (JV) measurements are obtained by using a Keithley Source Meter 2420 at room temperature and 1000 W/m^2.
Capacitance voltage (CV), drive level capacitance profiling (DLCP) and admittance spectroscopy (AS) measurements are carried out by a HP4284A LCR: the temperature is controlled by a Janis cryostat with Lakeshore 325 temperature controller, in a vacuum of 10^{-4} Pa and in a temperature range between 100 K and 320 K.
The crystalline structure and the compositional phases were analysed by grazing incidence X-Ray diffraction (GXRD) with a Philips vertical diffractometer with Cu-Kα radiation, and Goebel monochromator.
Accelerated stress tests (AST) were performed in a specific metal chamber, where a rack of halogen lamps and a temperature system control allows to keep the cells under one sun and 80 °C.
X-ray photoelectron spectroscopy (XPS) experiments were performed at the Stephenson Institute for Renewable Energy and Department of Physics, University of Liverpool, in a standard ultrahigh vacuum surface science chamber operating at a base pressure of 2×10^{-10} mbar. Core-level electronic structure was probed using a dual anode Mg Kα (1253.6 eV) X-ray source operating at 200 W and a hemispherical PSP Vacuum Technology electron energy analyser. The spectrometer was calibrated using Au 4f7/2 at 83.9 eV. XPS spectra were fitted using Voigt functions after Shirley background removal with an overall resolution of 0.2 eV.
High resolution TEM imaging was carried out in a FEI Tecnai F20 equipped with an Oxford Instruments X-Max 80 silicon drift detector (SDD) energy dispersive X-ray detector (EDX). The TEM analysis was performed in Loughborough University by Ali Abbas.
Deep level transient spectroscopy (DLTS) was performed with 1 V bias at the Stephenson Institute for Renewable Energy and Department of Physics, University of Liverpool, by Jon Major.

In our laboratory, CdTe cells are fabricated in superstrate configuration by low-temperature process based on vacuum evaporation (VE). The front contact consists of a 300 nm thick indium tin oxide (ITO) layer, followed by a 100 nm thick zinc oxide (ZnO) layer, both deposited by sputtering on a 4 mm thick soda lime glass. The stack is then annealed at 450°C in vacuum. A CdS layer about 100 nm thick is deposited by high vacuum thermal evaporation, at a pressure of 10^{-4} Pa and with a substrate temperature of 150°C. Then, an annealing in vacuum at 450°C is applied to favour the recrystallization of the layer. In the same chamber, a 7 μm CdTe layer is deposited by thermal evaporation, at a pressure of 10^{-4} Pa and with a substrate temperature of 340°C. Subsequently, the activation treatment is performed on the absorber: a $CdCl_2$ solution in methanol is applied by wet deposition, and the sample is heated at temperatures around 400°C. CdTe is then etched in a bromine-methanol solution, in order to remove the $CdCl_2$ residues but most important to form a p^+ tellurium rich layer. Immersing the sample in water is an alternative method to just remove the $CdCl_2$. The back contact is formed by a copper layer followed by a 30 nm thick gold layer, deposited by vacuum evaporation with the substrate at room temperature. In our samples, the optimum copper amount has been found to correspond to a 2 nm thick layer. In

this work, devices with a 0.1, 0.5 and 1.0 nm thick Cu layer have been also produced. Typically our standard complete devices are annealed in air at 200°C for 30 minutes in order to reach high efficiencies; in case of a 0.1 nm thick Cu layer, an additional annealing at 300°C is needed.

8.2.2 Performance of the devices

In order to study the effects of copper on the behaviour of our solar cells, we have changed its amount at the back contact, depositing the least possible quantity by evaporation, which is about (0.1 ± 0.05) nm. After the final annealing at 200°C, our standard devices with a 2.0 nm thick Cu layer reach efficiencies just below 16 %, while the 0.1 nm thick Cu layer samples reach low efficiencies from 1 to 6 %, mainly due to a low short circuit current, which in the best cases is around 12 mA/cm^2. It has been hypothesized that this low current is due to a potential barrier at the back contact or to a low doping of CdTe bulk. To increase the efficiency of these samples, an additional annealing at 300°C in vacuum is needed. In that way, efficiencies up to 14 % are obtained. On the other hand, this second annealing gives rise to a marked roll over in the current-voltage characteristic.
It is important to underline that our samples without intentional added copper do no exceed the 1 % of efficiency after the 200°C annealing, and the 4 % after the additional 300°C annealing. Probably in these samples the efficiency improvement is due to the Cu impurities present in the gold layer. However this demonstrates that a 0.1 nm thick Cu layer has a tangible impact on the devices.

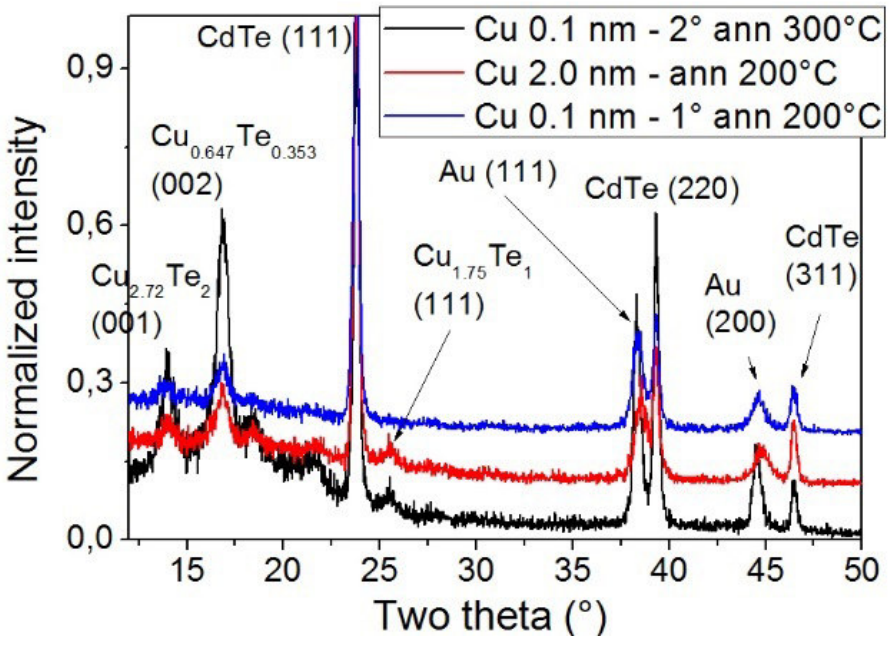

Figure 8.2.1: comparison of GXRD spectra of samples with a 2.0 nm thick Cu layer and with a 0.1 nm thick Cu layer after the annealing at 200°C and after the second annealing at 300°C.

In order to explore if the second annealing at 300°C influences the compounds at the back contact, lowering the potential barrier, GXRD spectra of samples containing a 2.0 nm thick

copper layer have been compared with the ones of 0.1 nm Cu samples after the first annealing at 200°C, and after the second at 300°C.
Actually, in figure 8.2.1, the sample with a 0.1 nm thick Cu layer after the 300°C annealing shows the same CuTe compounds of the 2.0 nm sample. On the other hand, the 0.1 nm sample after the 200°C annealing does not show the peak at 25.5°. Moreover, the annealing at 300°C lead to an intensity growth of the CuTe peaks at 14° and 16.8°. Considering the grazing geometry with the incidence angle fixed at 0.5° and the diffraction angle in the same scale, the penetration depth should be around 0.5 μm. For this reason, GXRD spectra suggest that the second annealing at 300°C favour the copper diffusion in the first layer of the CdTe. Possibly the higher temperature balances the lower concentration gradient due to the lower amount of material. Therefore with this minimum Cu amount a higher temperature is needed to sufficiently diffuse Cu into CdTe. Thus, the efficiency improvement after the annealing at the 300°C could be due to the lowering of the potential barrier. In fact, it is known that the Cu diffusion in the Te-rich layer (generated by etching) leads to the formation of Cu_xTe_{1-x} phases, which lowers the back contact barrier. Moreover Cu diffusion increases the carrier concentration in that region, producing a "p^+" layer which narrows the barrier, allowing the carriers to tunnel through it [12].

In order to compare devices with a wider range of copper thickness, also samples with a 0.5 nm and a 1.0 nm thick Cu layer have been fabricated. These kind of samples do not need the above-mentioned additional annealing at 300°C to reach high efficiencies.

Table I: average efficiency parameters of samples containing different amount of Cu: efficiency (η), fill factor (FF), open circuit voltage (Voc) and short current density (Jsc).

Cu amount (nm)	η (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
0.1	13.3 ± 0.6	64 ± 3	838 ± 21	25 ± 1
0.5	13.5 ± 0.4	66 ± 1	820 ± 12	25 ± 1
1.0	15.5 ± 0.3	71 ± 1	853 ± 10	25 ± 1
2.0	15.6 ± 0.3	71 ± 1	853 ± 10	26 ± 1

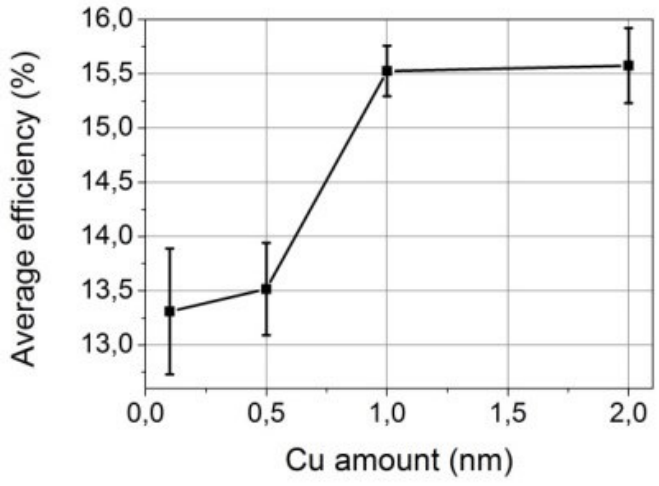

Figure 8.2.2: samples average efficiency versus Cu amount.

In table I the efficiency parameters of samples containing different amount of Cu are compared. Increasing the amount of Cu from 0.5 to 1.0 nm allows to obtain higher average FF around 71 %, and higher average Voc around 853 mV; this leads to higher efficiencies up to 16 %. The efficiency trend versus the Cu amount is represented in figure 8.2.2: where a net performance improvement is evidenced increasing the thickness of the Cu layer from 0.5 to 1.0 nm.

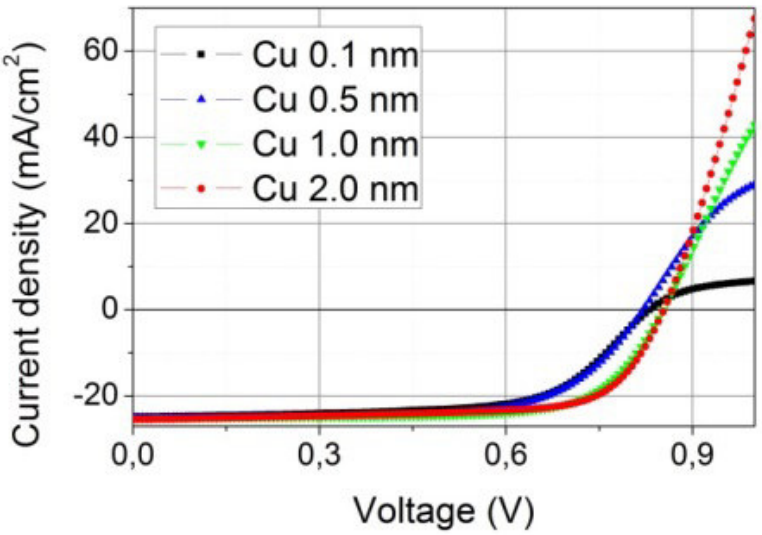

Figure 8.2.3: comparison of the JV characteristics of samples containing different amount of Cu.

In figure 8.2.3 the current-voltage characteristics of typical samples containing different amount of copper are compared. The samples with a lower copper content show a strong roll over, symptom of a higher back contact barrier, which explains the low fill factor. Increasing the copper thickness, the back contact barrier is decreased, allowing the fabrication of well performing devices.

8.2.3 The search of copper through TEM-EDX analysis

Our standard 2.0 nm thick Cu sample was submitted to TEM-EDX analysis in order to try to detect copper inside the device.
In figure 8.2.4: a TEM image of a samples containing a 2.0 nm thick Cu layer is shown. All the various layers of the device are clearly distinguishable, apart from the Cu layer, which is too thin.

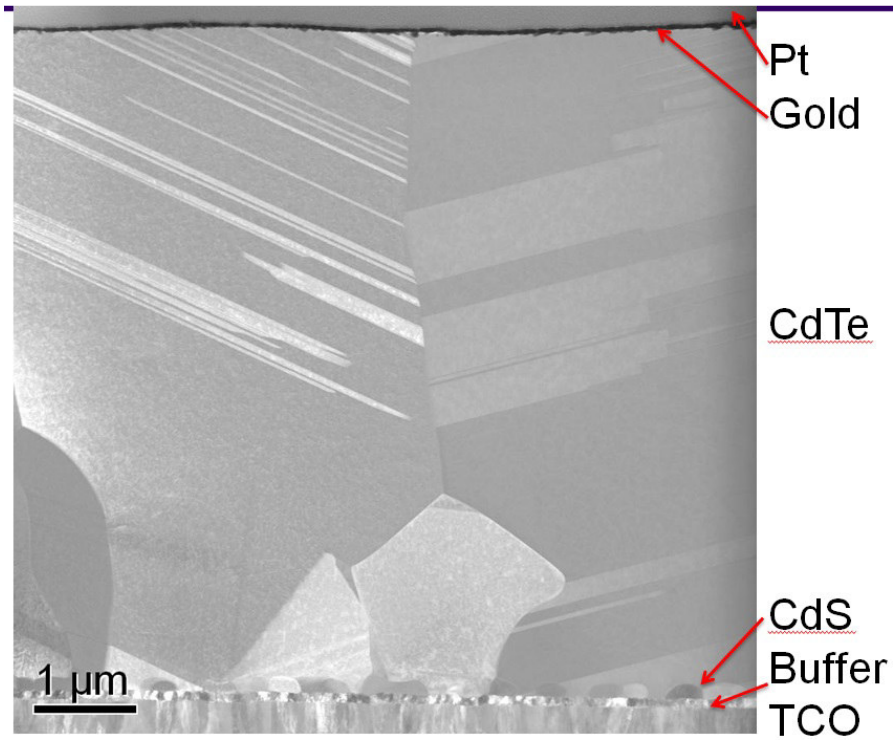

Figure 8.2.4: TEM image of our 2.0 nm sample.

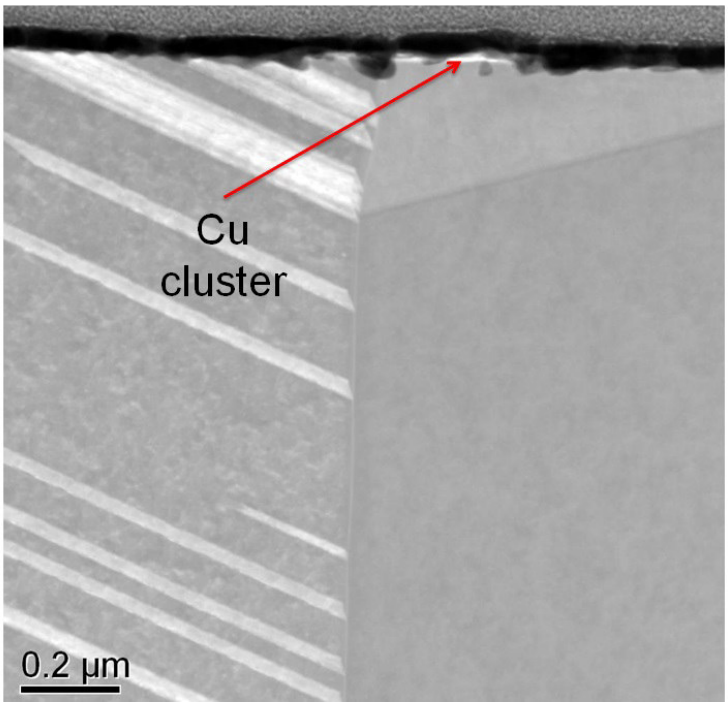

Figure 8.2.5: TEM image focused on the back contact of the 2.0 nm sample: it is possible to see a Cu cluster.

Form figure 8.2.5, which is a TEM image focused on the back contact of the 2.0 nm sample, it is possible to clearly see a copper cluster. On the other hand it is difficult to discern a homogeneous copper layer. The roughness of the CdTe surface is more than 2.0 nm depth, and for this reason it is quite impossible to clearly see a homogeneous thin Cu layer through scanning transmission electron microscope analysis.

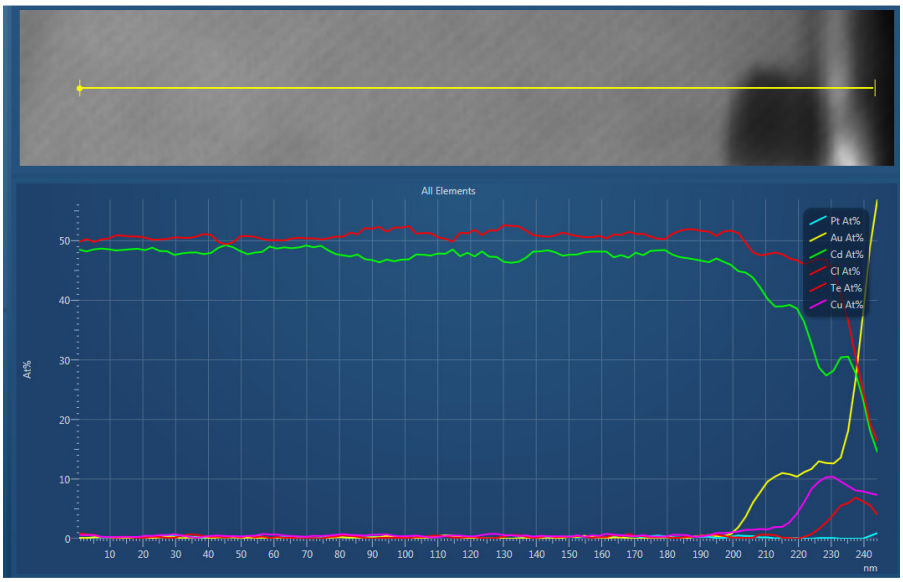

Figure 8.2.6: EDX maps of the back contact of the 2.0 nm sample: the gold contact is on the right.

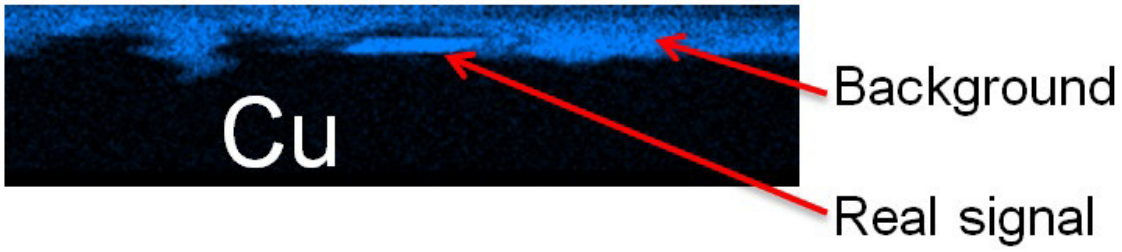

Figure 8.2.7: EDX map with high magnification of the copper contained in the back contact of the 2.0 nm sample.

The EDX maps of the elements present in the 2.0 nm sample are represented in figure 8.2.6, while the EDX map with high magnification concerning copper only is shown in figure 8.2.7. The main copper signal present in the figures is attributable to background in the gold layer. In figure 8.2.7 we can just see a copper cluster below the gold layer. In the absorber the Cu signal is below the instrument detection limit.
From these measurements I can conclude that the TEM-EDX analysis was not decisive to detect a so thin copper layer inside the sample. For this reason, no analysis were performed on samples containing a thinner copper layer.

8.2.4 Degradation mechanism of the devices

Copper is a fast diffuser in CdTe solar cells, and lot of studies have evidenced that its diffusion heavily influence the devices degradation [9,13-15]. It has been detected at the CdTe/CdS junction [12], where it can form recombination centres, moreover it can introduce shunt paths at the grain boundaries, which appear to be the most likely pathways for its diffusion [13,16].
To stabilize Cu at the back contact, different approaches have been proposed: for example the use of buffer layers that avoid Cu diffusion such as As_2Te_3 [17] and Bi_2Te_3 [18], the introduction of a ZnTe:Cu [1,19] back contact, or the formation of Cu_xTe compounds by CdTe surface etching followed by Cu deposition [20,21]. As mentioned in the devices fabrication section we use the latter method, etching the CdTe surface with a bromine methanol solution. In a previous work we have shown that etching duration (with a fixed solution concentration) heavily affects the stability of cells with a 2.0 nm thick copper layer [21]. To investigate the effect of the bromine-methanol etching on cells with the minimum amount of copper, they have been submitted to the same accelerated stress tests (AST) (described in the material and instrument section). Two set of 8 cells each have been fabricated with two different recipes: in the first CdTe has been 40 second etched in a bromine-methanol solution, while in the second no etching has been performed and the $CdCl_2$ residues have been removed with water. The two recipes lead to the fabrication of samples with the same average performance. Then, half the set has been aged in open circuit condition (OC), half in short circuit condition (SC) with front and back contact shunted, thus with current flowing. Their performance degradation has been analyzed by measuring their efficiencies at different time steps. The average efficiency of each half set during the AST is presented in figure 8.2.8.

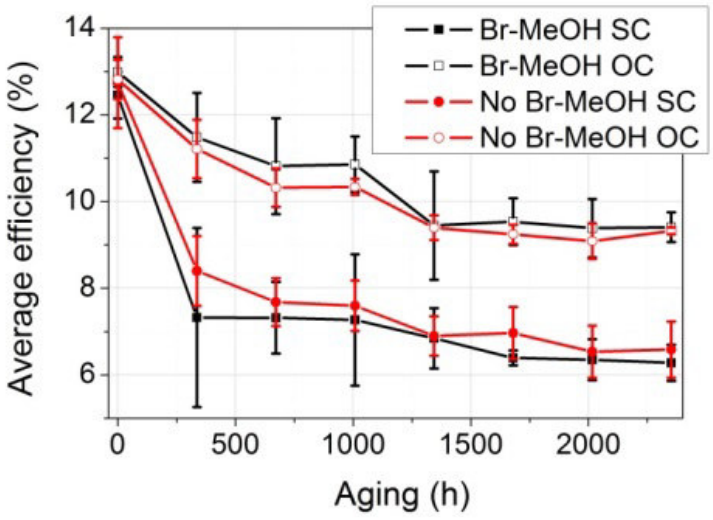

Figure 8.2.8: efficiency of samples with a 0.1 nm thick Cu layer, with and without bromine-methanol etching, aged in OC and SC condition, at different time steps of AST.

The acquired data show that bromine-methanol etching does not influence the stability of devices containing a 0.1 nm thick copper layer. In fact samples under the same aging

condition, which differ only from the etching, exhibit the same average degradation in time. This indicates that in case of samples with a 0.1 nm thick Cu layer, submitted to the additional annealing at 300°C, the etching is not functional to stabilize Cu at the contact.
It is also very interesting to note that samples aged in open circuit condition are more stable than the ones aged in short circuit condition. This will be discussed later.
In order to compare the copper compounds at the back contact of samples submitted or not to Br-MeOH etching, GRXD have been performed (see figure 8.2.9).

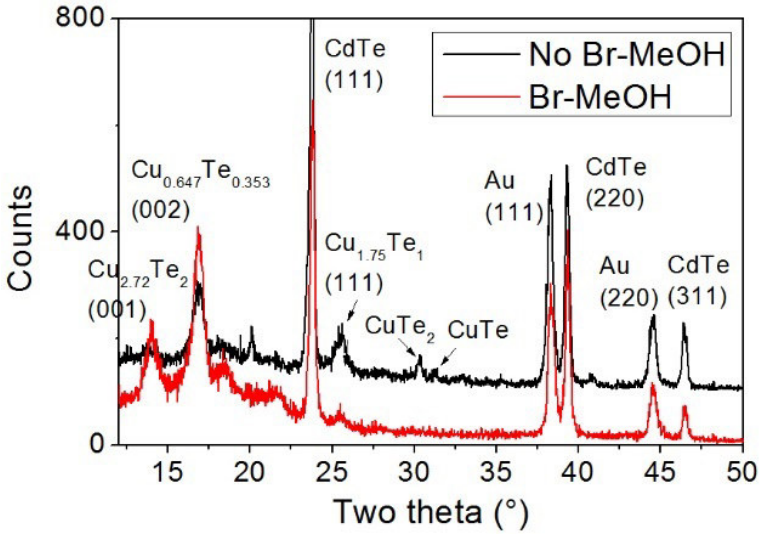

Figure 8.2.9: GXRD spectra of samples with a 0.1 nm thick Cu layer, with and without bromine-methanol etching.

Both samples show copper compounds at the back contact. Thus, CuTe compounds are formed even without Br-MeOH etching, but they are of different nature. However, with this minimum Cu amount, they do not affect the stability of the devices.

To compare the stability of these samples with the one of our standard samples, AST have been performed also on devices with a 2.0 nm thick Cu layer. The data are presented in figure 8.2.10, compared with those of 0.1 nm thick Cu layer's samples. In this case all the devices have been 40 second etched. To allow the comparison despite the different initial average performance, due to the different copper amount, normalized efficiencies are represented.

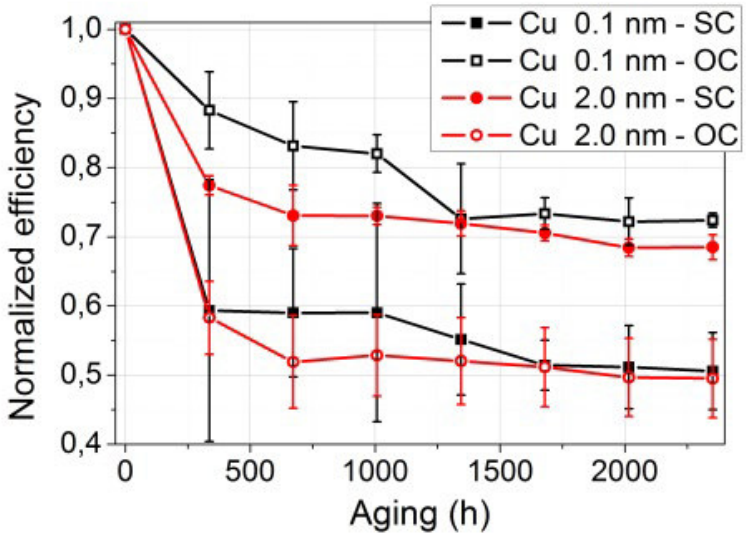

Figure 8.2.10: normalized efficiency of samples with 0.1 and 2.0 nm thick Cu layer, aged in OC and SC condition, at different time steps of AST.

On average, the samples with the minimum copper amount in OC show higher stability in the first 1000 hours of AST; after 2400 hours the 0.1 nm samples in OC are less degraded of 4 percentage points respect to the 2.0 nm samples in SC. We have already shown that the degradation of the samples is bias dependent, even in the presence of Cu_xTe compounds at the back contact [21]. What is surprising is the inversion of the bias dependency. Cells with a 0.1 nm thick Cu layer are more stable when aged in open circuit condition, while generally, in samples with Cu intentionally added, the degradation effects are larger in open circuit condition [9-12]. In this case, different degradation mechanisms predominate in cells with different copper amount. This phenomenon can help understand the behavior of copper inside the devices.

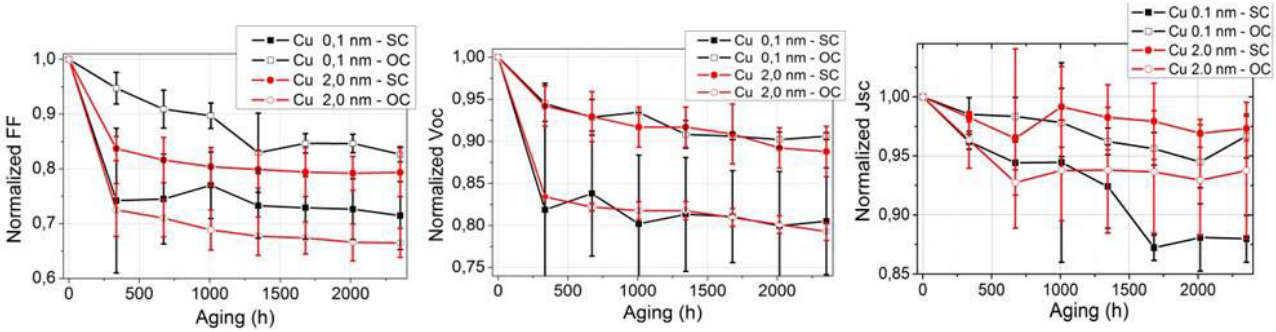

Figure 8.2.11: normalized FF (left), Voc (center) and Jsc (right) of samples with 0.1 and 2.0 nm thick Cu layer, aged in OC and SC condition, at different time steps of AST.

In figure 8.2.11 the normalized FF, Voc and Jsc of the same samples of fig. 8.2.10, at different time steps during the AST, are represented. The fill factor is the main responsible of the degradation of the devices, followed by the Voc. On the other hand, the Jsc has lower influence on the performance drops.

To understand more accurately between which Cu thicknesses the inversion of the bias dependency occurs, also samples with a 0.5 and 1.0 nm thick Cu layer have been submitted to AST.

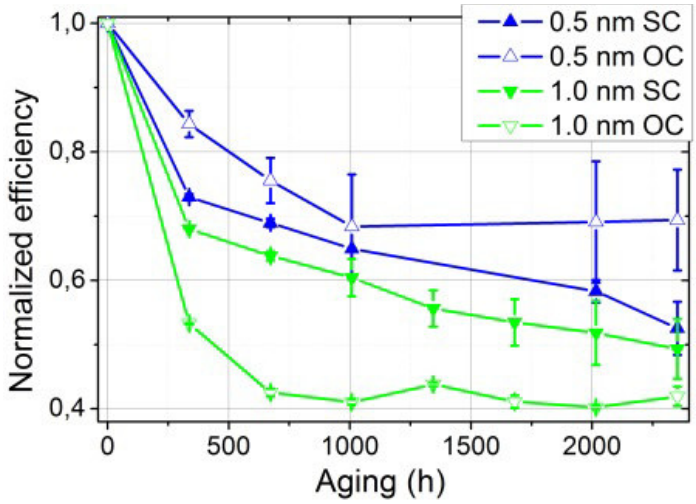

Figure 8.2.12: normalized efficiency of samples with 0.5 and 1.0 nm thick Cu layer, aged in OC and SC condition, at different time steps of AST.

Samples with a 0.5 nm thick Cu layer are more stable when aged in OC condition (see figure 8.2.12), while 1.0 nm samples are more stable in SC condition. Thus the inversion takes places between 0.5 nm and 1.0 nm, that is also when a net performance improvement occurs (see figure 8.2.2).
As the 0.5 nm samples have not been submitted to the additional annealing at 300°C, the different aging mechanism is not strictly related to the annealing temperature.

In order to better understand if the copper thickness influences the degradation mechanism through the formation of different compounds on the surface of the CdTe, XPS measurements have been performed on samples with a 0.1, 0.5, 1.0 and 2.0 nm thick Cu layer. All samples were prepared with a 5 nm thick gold layer on top, to allow the analysis.

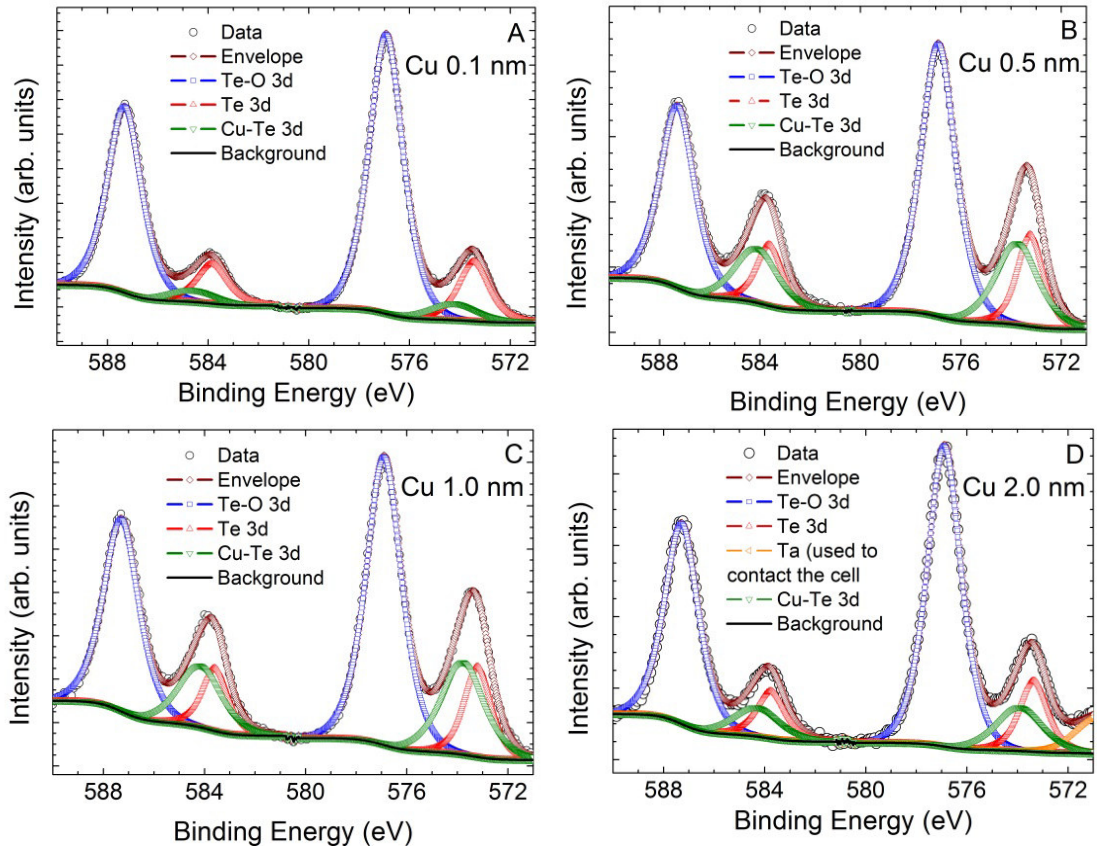

Figure 8.2.13: XPS spectra of finished devices containing a different copper amount: A) 0.1 nm, B) 0.5 nm, C) 1.0 nm, D) 2.0 nm.

The XPS spectra (reported in figure 8.2.13) highlight the presence of the same compounds regardless the thickness of the copper introduced. All the samples show the presence of tellurium and tellurium oxides, and most important, of cupper telluride compounds. Unfortunately it is not possible to make a quantitative comparison, because the height of the peaks is strongly influenced by the slight difference in thickness of the gold layers. However it is possible to conclude that also in the case of the minimum copper amount, and after two annealing at 200° C and 300°C, copper is still present on the surface forming CuTe compounds.

8.2.5 Doping and identification of the defects

It is important to understand the effects of the different copper amount on the CdTe doping. A reduced Cu quantity would suggest a lower doping. With capacitance voltage (CV) and drive level capacitance profiling (DLCP) measurements the net charge density in CdTe of acceptor-minus-donor states can be estimated as a function of distance from the junction. The net charge density is determined from the lower part of the U-shape profile in order to avoid effects due to others factors, such as a not perfectly ohmic back contact or the limited thickness of CdTe [22]. The CV profiles (indicated in figure 8.2.14 with open dots) show the contribution of both deep and shallow defects, while the deepest states hardly affect the

DLCP curves (full dots), so the difference between each pair of curves is associated to the presence of deep states [23].

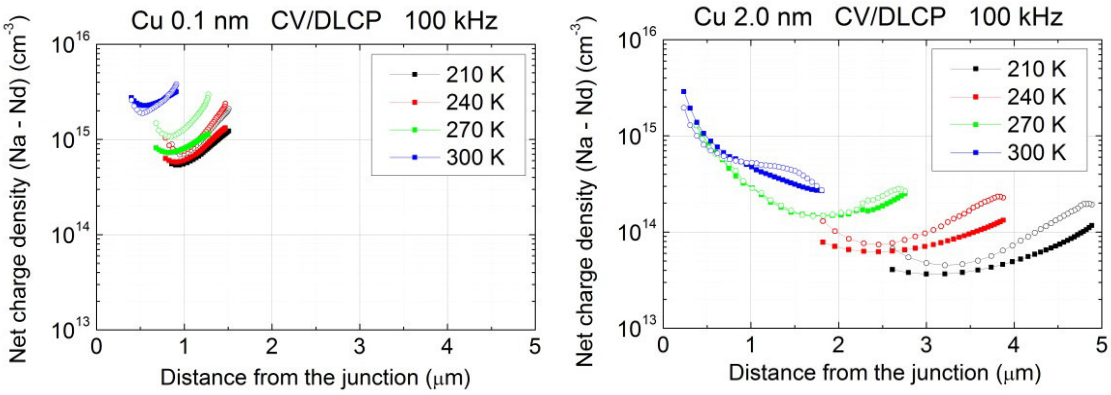

Figure 8.2.14: comparison between CV (open dots) & DLCP (full dots) measurements of samples containing a 0.1 nm (left) and 2.0 nm (right) thick Cu layer.

At the frequency of 100 kHz the 2.0 nm sample shows a net charge density lower of about an order of magnitude compared to the 0.1 nm sample: in particular at 300 K the values are 3 * 10^{14} versus 2 * 10^{15} cm^{-3}. This implies also a wider depletion region, as confirmed by fig. 8.2.14. Moreover the 2.0 nm sample profile is more temperature dependent that the 0.1 nm sample one: as the temperature rises, in the 2.0 nm case (fig. 8.2.14, right side) the net charge density increases constantly with temperature, while in the 0.1 nm case (fig. 8.2.14, left side) the main increase happens between 270 K and 300 K. The same analysis has been done also at frequencies of 10 kHz and 1 MHz (not shown here), with similar results. The main difference is that in the 0.1 nm sample, at 10 kHz, the main net charge density increase happens between 240 K and 270 K. While the 2.0 nm sample does not show dependence on the frequency of the measurement. All that indicates that the dominant defects are of different nature in the two samples, however both kind of samples show the presence of deep defects.
It is quite surprising that the 0.1 nm sample shows a higher net charge density, despite the lower amount of copper and the lower efficiency achieved. This suggests that this minimum copper quantity is enough to dope a 7 μm thick CdTe layer. Possibly a larger copper amount creates a larger number of donor defects which compensate the doping due to the Cu itself [6-8]. As a 0.1 nm thick Cu layer is enough to dope the absorber properly, the lower efficiency achieved by the 0.1 nm samples could be totally due to the poor ohmicity of the back contact, so to the lack of Cu between CdTe and gold.

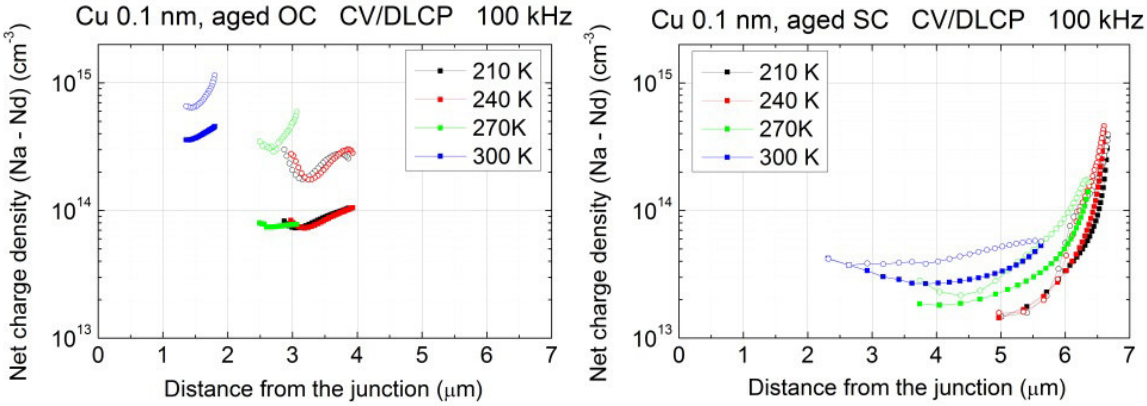

Figure 8.2.15: comparison between CV (open dots) & DLCP (full dots) profiles of samples containing a 0.1 nm thick Cu layer, submitted to 335 h of AST in OC (left) and SC (right) condition.

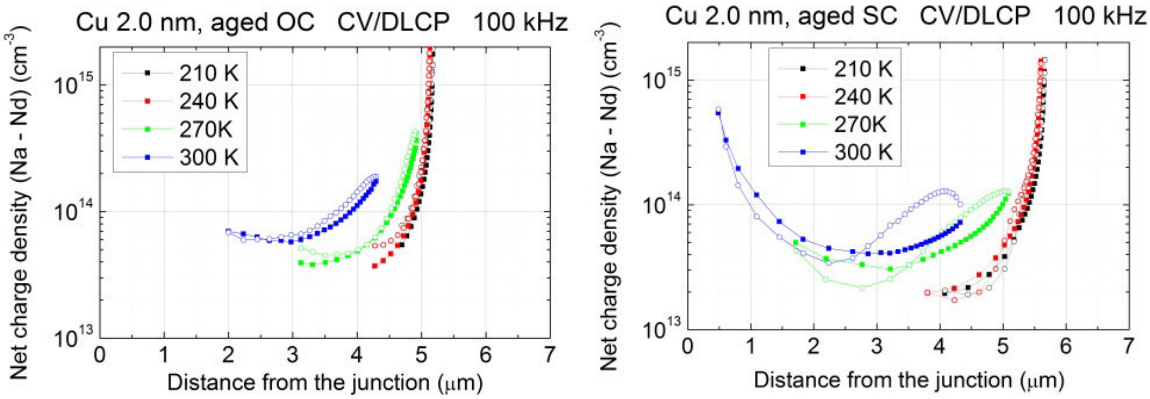

Figure 8.2.16: comparison between CV (open dots) & DLCP (full dots) profiles of samples containing a 2.0 nm thick Cu layer, submitted to 335 h of AST in OC (left) and SC (right) condition.

In order to interpret the efficiency degradation mechanism revealed by AST, the CV DLCP profiles of the 0.1 nm sample (figure 8.2.15) and of the 2.0 nm sample (figure 8.2.16) after 335 h of aging in OC and SC condition are also presented. As expected the net charge density of all the samples aged both in OC and SC condition drops. Moreover the profiles at lower temperatures of all the samples, apart from the 0.1 nm aged in OC case, increase in the right part of the graph. This effect is the influence of the back contact and it reveals that the depletion region extends too close to the contact, as a consequence of the poor net charge density. The 0.1 nm aged in OC sample shows the higher net charge density, and at the same time a large amount of deep defects. As before the AST, the 2.0 nm samples reveal a lower net charge density. Possibly a higher amount of Cu diffusion from the back contact leads to the formation of a larger amount of compensating defects, in fact, an excessive Cu diffusion can compensate the Cu_{Cd}^{-} acceptors with Cu_i donors [6-8]. The net charge density drops in the 0.1 nm aged in SC sample is not of easy interpretation: in some way the current flow during the AST seems to damage the acceptor states present in the device.

To explore the nature of the different defects, seen by CV-DLCP measurements in samples with different Cu amount, deep level transient spectroscopy analysis was performed. DLTS measurements allow to estimate the activation energy (E_a) above the valence band, the cross section (σ_a) and the concentration (N_t) of the dominant traps (see table II). The analysis has been focused on the 80-250 K temperature range, under 1V bias condition. At higher temperature it is difficult to make an accurate analysis because the influence of the back contact can begin to overlap the data leading to errors.

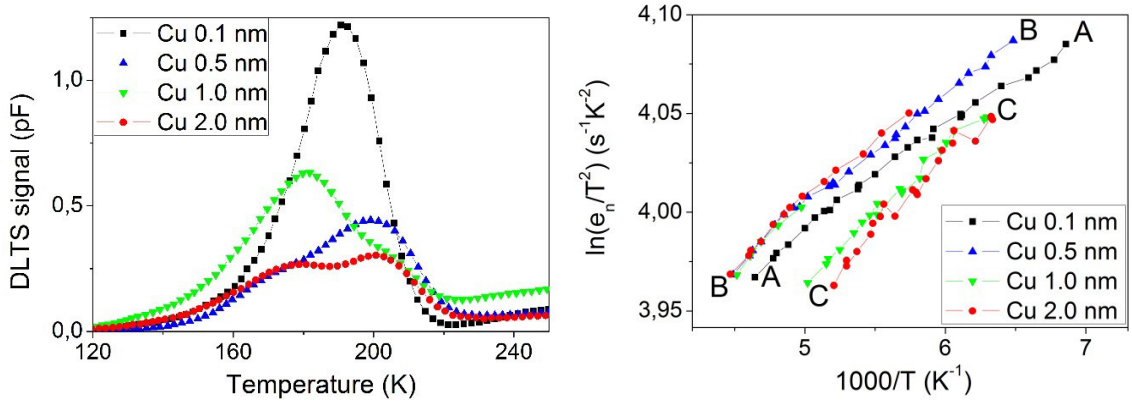

Figure 8.2.17: DLTS of samples with different Cu amount (left): temperature scan and 1 V applied bias. Arrhenius plot (right) of deep levels in the samples: the signatures are given in table II.

Table II: Activation energy above the valence band, cross section and concentration of deep levels in the samples, derived from the Arrhenius plot of fig. 8.2.17.

Samples	Defects								
	A			B			C		
Cu in samples	E_a (meV)	σ_a (cm^2)	N_t (cm^{-3})	E_a (meV)	σ_a (cm^2)	N_t (cm^{-3})	E_a (meV)	σ_a (cm^2)	N_t (cm^{-3})
0.1 nm	242	$4 * 10^{-18}$	$7 * 10^{12}$						
0.5 nm				275	$1 * 10^{-17}$	$3 * 10^{12}$			
1.0 nm				283	$2 * 10^{-17}$	$3 * 10^{12}$	318	$1 * 10^{-15}$	$5 * 10^{12}$
2.0 nm				276	$1 * 10^{-17}$	$2 * 10^{12}$	344	$1 * 10^{-14}$	$2 * 10^{12}$

On the left side of fig. 8.2.17, DLTS of samples containing a 0.1, 0.5, 1.0 and 2.0 nm thick Cu layer are presented, moreover the Arrhenius plot extracted from the analysis are shown on the right. In the 0.1 nm Cu sample a single dominant level at 242 meV above the valence band seems to be present. In all other samples a pair of dominant levels are identified, although these are difficult to separate for the 0.5 nm sample, because they show a similar E_a. The obtained values are 275-283 meV (level B) and 318-344 meV (level C) above the valence band. In order to make an assessment of the validity of the results, given the identified levels, by using the simulation package it is possible to generate the expected DLTS spectra (not shown here). Obviously this is then compared to the initial DLTS. The extracted values give a good fit for the 0.1 nm sample, and a reasonable outcome for the

others. For these samples the fitting can be improved by including level A determined from the 0.1 nm sample, although this can not specifically be resolved in these samples. For this reason a valid assumption is that the A level is present in all samples, but it can not be resolved due to the presence of the B and C levels. We hypothesize that the A level is Cl-related, while B and C levels are generated by copper addiction. Other authors have previously identified trapping levels similar to B and C [24], deducting a donor nature of that levels. This is in good agreement with our observation based on the CV DLCP measurements. In fact CV DLCP profiles (fig. 8.2.14) suggest the formation of donor defects with the increase in the copper amount, which reduce the net charge density of acceptors minus donors in the samples. In other words, the defects identified by DLTS measurements could explain the higher net charge density in samples containing a lower copper amount. For these reasons, the previous measurements suggest that the lower efficiency of samples containing a lower copper amount is not due to an insufficient CdTe doping.

8.2.6 Discussion

Samples containing a 0.1 nm thick copper layer can reach efficiencies just below 14 %, which is about two percentage point below the average efficiency of our standard samples containing a 2.0 nm thick Cu layer. To achieve these efficiencies, samples with this minimum Cu amount need an annealing of the finished device at 300°C, in addition to the standard at 200°C. Probably the higher temperature balances the lower concentration gradient due to the lower amount of material, thus a higher temperature is needed to sufficiently diffuse Cu into CdTe. This is confirmed by the comparison of GXRD spectra of samples after the 200°C annealing, and after the additional 300°C annealing, which reveal a larger amount of copper (and more similar to the 2.0 nm sample) at a depth around 0.5 µm after the second annealing.
With a 0.1 nm thick copper layer, Br-MeOH etching does not influence the stability of the samples, moreover GXRD spectra reveal the presence of CuTe compounds even without the etching. Possibly the native Cd vacancy are enough to form CuTe compounds, and to influence the diffusion of such a small quantity of Cu. Furthermore, CuTe compounds are detected from XPS measurements on CdTe surface, even in the 0.1 nm sample.
Regarding CdTe doping, the CV DLCP measurements highlight a net charge density of an order of magnitude higher in the sample with a 0.1 nm thick Cu layer compared to our standard sample. Consistently, DLTS measurements detect the presence of a single defect in the 0.1 nm case, possibly chlorine related, and of two additional donor defects with the increase of the copper amount in the devices. This suggests that a 0.1 nm thick Cu layer can dope a 7 µm thick CdTe layer, as also deduced by Kranz et al. [6] for substrate configuration devices, while the additional copper amount leads to the formation of compensating defects.
Actually, the fill factor is the main parameter which negatively affects the J-V characteristics of the 0.1 and 0.5 nm samples. It is clearly caused by a marked roll over, symptom of a high back contact barrier. In the 0.1 nm case, a strong increase of the roll over is denoted after the second annealing, highlighting that it is related to the Cu diffusion from the contact. Thus, despite copper succeeds in forming CuTe compounds, this thickness is insufficient to favor the perfect ohmicity of the contact between CdTe and gold. Moreover, our samples do not work properly without Cu, and it has been already simulated that for absorber layer thicker than 3.5 µm, the direct contact between CdTe and gold lead to the formation of a marked roll over [25].

This work discloses that the degradation mechanism of CdTe solar cells depends on the copper amount. In fact accelerated stability tests show that samples containing a copper layer up to 0.5 nm thick are more stable in open circuit aging condition, while samples containing a 1.0-2.0 nm thick Cu layer are more stable in short circuit aging condition. A surprising inversion of the bias dependency happens between 0.5 and 1.0 nm, which is also the range in which the average efficiency increases from 13.5 % to 15.5 %. This referred to a 7 μm thick CdTe layer.

As mentioned above Cu is a fast diffuser in CdTe solar cells, and its diffusion heavily influence the devices degradation [9,13-15]. An uncontrolled copper diffusion is widely considered the main cause of degradation of CdTe devices. Cu can segregate into the grain boundaries causing shunt paths [13,26]. In fact experiments suggest that Cu diffuses and accumulates preferentially along grain boundaries [13,16], where it is energetically favored according to first principles calculations [27]; this has also been confirmed by TEM studies [28]. On the other hand Cu can dope CdTe through the formation of Cu substitutional impurities Cu_{Cd}, but it can also form deep donor interstitial Cu_i defects, moreover it can form other complexes such as $Cu_{Cd}Cu_i$ [29,30]. It has been experienced that an optimum Cu amount leads to more performing devices, while an excess or a deficiency of copper in the cells damage the performance [13,31-33]. Relating the devices efficiency to the doping level of the absorber, the model proposed by Chin et al. [8] and Ma et al. [34] can explain this phenomenon. According to them, there is a maximum net charge density obtainable, which depends on the concentration of Cd vacancy in the deposited film, which affects the formation energy of the Cu_i and Cu_{Cd} defects.

Thus, possibly, a higher amount of Cu diffusion from the back contact leads to the formation of a larger amount of compensating defects, as an excessive Cu diffusion can compensate the Cu_{Cd}^- acceptors with Cu_i donors [6-8].

In the samples the copper diffusion is due to the concentration gradient and it can be affected by the presence of electric fields. Corwine et al. have assumed that much of the Cu at the back contact is in form of a positive ion, and for that reason the primary junction field of the cell resists the migration away from the contact [12]. Then, when a sample is exposed to light in open circuit condition, the formation of electron-hole pairs increases the drift current, consequently decreasing the build in potential at the junction [35]. This favors the diffusion of copper ions towards the junction. On the contrary, in short circuit condition the photo-generated current flows through the device; supposedly electrons and holes recombine with each other. Moreover we can imagine a flux of electrons coming from the back contact which opposes the ionic form of Cu atoms. This explains why, as mentioned above, generally in samples with Cu intentionally added, the degradation effects are larger in open circuit condition [9-12]. Moreover this explains the behavior of the 0.1-0.5 nm cells submitted to AST in OC condition, where the higher stability is due to the lower Cu diffusion towards the junction, simply given by the lower amount of copper added to the devices. However in the 0.1-0.5 nm samples aged in SC condition another degradation mechanism predominates; in fact both the concentration gradient and the bias lead these samples to be the ones with the lowest copper diffusion from the back contact. In this case the net charge density decrease (see fig. 8.2.15) could be associated with the migration of Cu atoms from Cd sites to interstitial sites [36]. The decay of the Cu_{Cd} acceptor into the donor acceptor pair Cu_i V_{Cd} has been previously observed [37,38]. Moreover this phenomenon is more evident in illuminated samples [37], thus it could be possibly influenced by the current flow in the sample.

Generally, at elevated temperature the solubilities for Cu and defect formation energies

change, triggering a redistribution of Cu and related defects [36]. Thus we speculate that in SC condition the current flow enhances the instability of the Cu_{Cd} acceptor states. Furthermore, it is possible that in the 0.1 nm case, the poor presence of interstitial copper and of copper diffusion from the contact makes the formation of others Cu_{Cd} states unlikely.

8.2.7 References

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8.3 $CuCl_2$ back contact

Polycrystalline CdTe devices are partly limited by low doping concentrations, primarily due to the lack of a dopant with both high solubility and shallow acceptor level [1]. One of the ongoing challenges of the technology is to produce a good quality and stable ohmic contact, because of the high CdTe electron affinity [2].
The standard solution has been the insertion of copper at the back contact, which reduces the Schottky barrier via formation of Cu_xTe_{1-x} phases and increased carrier concentration. This produces a "p^+" layer at the near back surface which allows carriers to tunnel through the barrier [3]. The mechanism of Cu doping for CdTe has been widely studied [4-6] and utilized in a variety of manners such as via simple copper evaporation or via inclusion in buffer layers at the back surface [7-11].
Whilst there has been some success with copper-free back contacts in the past, delivering efficiencies up to 15% [12,13], it is generally considered that copper is necessary to attain higher efficiency devices.

The use of copper in CdTe remains problematic however given it is a fast diffuser in CdTe and leads to performance degradation of the cells in the long term. Cu has previously been

detected at the CdTe/CdS interface [14], and at the CdS/CdTe junction forming recombination centers and shunt pathways [15]. For this reason different approaches have been applied to stabilize Cu at the back contact: such as the formation of Cu_xTe compounds by CdTe etching and subsequent Cu deposition [7,16], or the use of buffer layers such as As_2Te_3 [17] and Bi_2Te_3 [18] in order to avoid copper diffusion, or the development of a ZnTe:Cu back contact [19].

In this sub-chapter I analyze copper inclusion via a $CuCl_2$-Methanol solution. This process allows reduction of the incorporated copper quantity without any loss in performance compared to a standard Cu contacting route and simple and rapid depositing evenly over the entire area of the sample. Use of a chloride compound was chosen because due to the well-known chlorine related benefits of recrystallization, grain growth [20-22], and p-type doping (bicomplexes with native defects) [20,23] in CdTe.
Beach et al. suggested that the defects induced by $CdCl_2$, probably Cl-induced donor, increased the solubility of the Cu at Cd substitutional sites impurities Cu^-_{Cd}, which are considered acceptors [24].
The $CuCl_2$ is applied after the standard $CdCl_2$ activation treatment since combining activation treatment and copper doping in a single step is not possible: $CdCl_2$ activation treatment is applied at a temperature which would cause a very large Cu diffusion.
The results of this copper chloride wet deposition method (CCWD) on CdTe are the following:

i) Less Cu required to achieve peak performance: with amount of copper solution which is the equivalent of a 0.1 nm thick evaporated layer, JV characteristic shows a good ohmic back contact without roll over.

ii) Scalable deposition process where copper content can be easily controlled by tuning its concentration in methanol solution.

iii) Improved stability: proved by accelerated aging tests performed at an illumination of one sun and at a temperature of 80°C.

8.3.1 Experimental procedure

Current density-voltage (JV) characteristics were measured with a Keithley Source Meter 2420, using a halogen lamp calibrated with a silicon solar cell under an irradiation of 100 mW/cm^2 (AM 1.5).
Drive level capacitance profiling (DLCP), capacitance voltage (CV) and admittance spectroscopy (AS) are carried out by a HP4284A LCR. The temperature is controlled by a Janis cryostat with Lakeshore 325 temperature controller in a vacuum of 10^{-4} Pa and in a range between 100 K and 320 K.
The external quantum efficiency (EQE) was obtained at Department of Information Engineering, University of Padova, using a commercial LOANA solar cell analysis system, calibrated with a silicon reference sample with known EQE using an incident spotlight of 1 mm x 2 mm area.
The crystalline structure and the compositional phases were analysed by X-Ray diffraction (XRD) with a Philips vertical diffractometer with Cu-Kα radiation, and Goebel monochromator.

SIMS depth profiles were obtained at Department of Physics and Astronomy "G. Galilei", University of Padova, on a CAMECA IMS-4 f using an O_2^+ primary ion beam at a 12.5 kV accelerating voltage (corresponding to 8 keV impact energy) and detection of positive secondary ions. A mass resolution m/Δm ≈4000 was employed in the spectrometer to avoid mass interference between the $^{63}Cu^+$ and the $^{126}Te^+$ signals.
X-ray photoelectron spectroscopy (XPS) experiments were performed at Stephenson Institute for Renewable Energy and Department of Physics, University of Liverpool, in a standard ultrahigh vacuum surface science chamber operating at a base pressure of 2×10^{-10} mbar. Core-level electronic structure was probed using a dual anode Mg Kα (1253.6 eV) X-ray source operating at 200 W and a hemispherical PSP Vacuum Technology electron energy analyser. The spectrometer was calibrated using Au 4f7/2 at 83.9 eV. XPS spectra were fitted using Voigt functions after Shirley background removal with an overall resolution of 0.2 eV
For TEM-EDX analysis a JEOL 2100F microscope with CEOS probe corrector was used that was operated in scanning transmission electron microscopy (STEM) mode to acquire simultaneous high angle annular dark-field (HAADF) images, i.e. Z-contrast images, together with EDX element maps. A focused ion beam (FIB) in-situ lift-out method was used for cross-sectional TEM specimen preparation. TEM-EDX analysis were performed at Department of Materials Science and Engineering,
University of Michigan.

CdTe thin film solar cells are made in superstrate configuration by a low-temperature fabrication process based on vacuum evaporation (VE). A 100 nm thick CdS thin film is deposited at 150 °C on an ITO/ZnO 3x3 cm coated soda lime glass and subsequently annealed in vacuum at 450 °C. Then a 7 μm thick CdTe layer is deposited in the same vacuum chamber. The stack is activated by the $CdCl_2$ treatment, consisting of deposition which is applied by wet deposition, and annealed in air at 380 °C.
Prior to the back contact deposition, the CdTe surface is etched by a bromine/methanol solution in order to remove $CdCl_2$ residues and to generate a Te-enriched layer and allow the formation of a Cu_xTe compound.
In our standard process, back contact is made by thermal evaporation of a 2.0 nm thick copper layer followed by a 30 nm thick gold layer; annealing in air at 200°C of the finished device is needed to reach good efficiencies.
The CCWD process for CdTe consists of depositing on top of the CdTe layer a solution made of $CuCl_2$ powder diluted in methanol, typically 0.1 g of $CuCl_2$ per litre of methanol. An annealing of the stack at 200 °C for 30 minutes is applied to allow a chemical reaction between the bulk and the solution. Finally a 30 nm thick gold contact is deposited on free back surface.
In order to compare the CCWD with the VE process, we have deposited on top of the CdTe surface an amount of $CuCl_2$ solution, which is equivalent to a copper layer with a thickness of 0.1 nm. This has been calculated by comparing the amount of copper in the laid out solution with the value obtained by multiplying the copper volume of the thin evaporated layer by its density.
Practically 0.4726 μg of copper have been deposited on an area of 4.5 cm^2 of a 7 μm thick CdTe. Calculating the amount of copper atoms from its atomic mass we have about $1 * 10^5$ atoms /cm^2 near to the $0.8 * 10^5$ atoms/cm^2 indicated by Kranz et al. [6].

8.3.2 Performance of the devices

A large number of samples have been fabricated with CCWD step process, where the amount of used solution ranged from 10 to 20 µl, while annealing temperature was optimized at 200°C. Also, optimization of both $CdCl_2$ treatment and CCWD step were done together in order to achieve the best combination in terms of performance. In this way more than 50 samples, with 10 solar cells each of 0.13 cm^2 were produced with the new step process. These devices have been compared with samples using either a 2 nm or 0.1 nm VE-Cu contacting process. This last one has a very similar copper quantity of the CCWD cells, but deposited by vacuum evaporation and without chlorine. In order to avoid the performance degradation effects due to copper diffusion, one option could be to minimise the amount of copper applied, but this would reduce the performance, due to lower CdTe doping and to a higher back contact barrier.

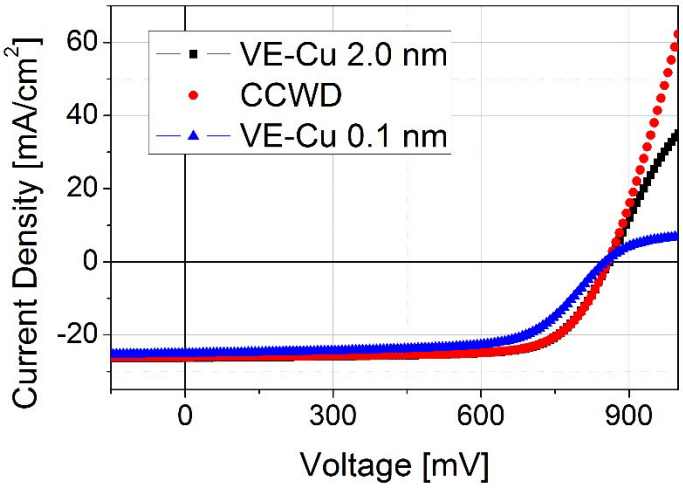

Figure 8.3.1: comparison between J-V characteristics of devices with 2.0 nm and 0.1 nm thick copper layer by evaporation (respectively black and blue), and with the equivalent amount of a 0.1 nm thick copper layer by wet deposition (red).

Figure 8.3.1 shows J-V characteristics of three of our best devices obtained inserting copper by evaporation and by wet deposition. Clearly, reducing the amount of evaporated copper from 2 to 0.1 nm, the conversion efficiencies reduce as expected (see Table 8.3-I). The reduction is mainly caused by a fill factor (FF) loss concurrent to a pronounced rollover. On the other hand, if the equivalent of 0.1 nm thick copper layer is inserted by CCWD on the CdTe, the series resistance is reduced and fill factor largely increases and conversion efficiencies are comparable to the ones of devices with 2 nm thick back contact layer. This is quite interesting because it proves that a very small amount of copper (see section 8.3.2) is sufficient for CdTe doping as reported by Kranz et al. [6]. However it is very important how and where the Cu is blended in the CdTe matrix, avoiding agglomeration at grain boundaries.

Table 8.3-I: efficiency parameters of devices of Fig. 8.3.1: conversion efficiency (η), fill factor (FF), open circuit voltage (Voc) and short circuit current density (Jsc).

Copper quantity	η (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
$CuCl_2$	15.9	73.1	859	25.4
2.0 nm	16.1	72.0	866	25,8
0.1 nm	13.8	66.0	852	24.5

Table 8.3-II: average efficiency parameters of devices.

Copper quantity	η (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
$CuCl_2$	15.7 ± 0.3	71.4 ± 1.4	852 ± 5	25.8 ± 0.3
2.0 nm	15.9 ± 0.1	71 ± 1.3	852 ± 10	26.4 ± 0.7
0.1 nm	13.8 ± 0.2	66.2 ± 0.8	847 ± 2	24.6 ± 0.5

Looking at table 8.3-II, the average performance parameters show that samples containing a 0.1 nm thick copper layer deposited by CCWD reach almost the same average efficiency (η) than samples containing a 2.0 nm thick copper layer deposited by vacuum evaporation (VE-Cu). In particular the average fill factor of CCWD samples is slightly larger which is quite surprising considering the small amount of Cu.
The choice of $CuCl_2$ as Cu carrier has been done according to the well-known effects of chlorine-based treatments, enhancing a chemical reaction with CdTe [25], generating a rearrangement of the CdTe structure and reducing the grain boundaries' effect. However, the results show that inserting copper by chlorine carrier improves the back contact, but it can not be excluded that it also might change the interface and the bulk structure of the absorber. In order to clarify this aspect, an analysis of the spectral response of two different cells, with efficiencies around 13%, have been pursued by External Quantum Efficiency measurements (see figure 8.3.2), performed on CCWD and VE-Cu samples. EQE responses of the different cells do not show significant differences; attesting that CCWD does not influence band gap or carrier lifetime. Similar response for different cells at long-wavelength region show that the CdS_xTe_{1-x} intermixed layer has not been modified by the additional chlorine treatment; as it is known that the formation of an intermixed layer reduces the band gap [26], shifting the EQE response.
An improved response is observed in the range of 600-750 nm, in the wavelength range absorbed in a more distant zone from the junction. This suggests that CCWD absorber shows a larger mean free path of the carriers.

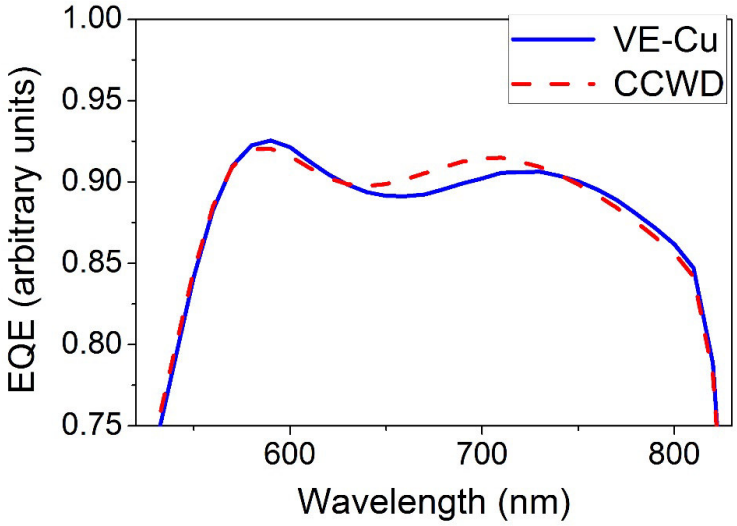

Figure 8.3.2. Detail of EQE spectra for the two different samples: a slight increase in response is observed for the CCWD case.

8.3.3 Structural analysis

The activation treatment, with $CdCl_2$, is typically changing the grain structure of the absorber, in particular is affecting both shape (and size in case of low temperature deposited CdTe) and orientation of the grains [27].
Thus it is interesting to verify if CCWD process would also modify the structure of the CdTe bulk, due to the presence of chlorine. For this reason, XRD patterns have been acquired on the surface of the completed VE-Cu and CCWD photovoltaic devices (see figure 8.3.3), considering that in the standard geometry the x-rays are able to penetrate more than 0.5 μm in the stack.
As shown in figure 8.3.3, CdTe peaks are present in both samples, as expected. The main difference among them is that the CCWD sample reveals a CuO peak, while on the other hand the VE-Cu sample shows a different peak, which is attributable to Cu. This is easily explained by considering that when Cu is deposited by thermal evaporation, final annealing of the stacks is applied after Au deposition avoiding Cu oxidation. This is not the case for CCWD where the annealing is applied in air, before Au deposition giving place to possible oxidations.

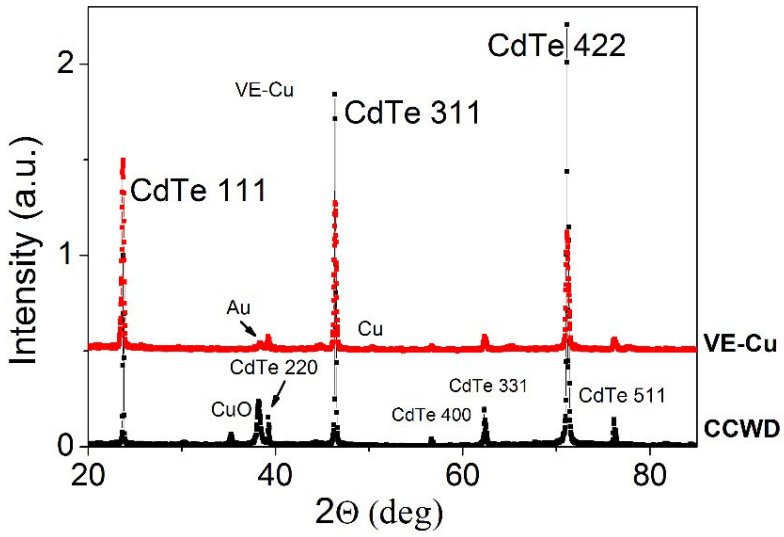

Figure 8.3.3: XRD spectra of Cu and $CuCl_2$ finished devices.

Moreover we can observe a slightly different recrystallization for the CCWD case, where the preferential orientation of the (111) peak is completely lost in favour of the (422) orientation. In particular for the VE-Cu case (111)>(311)>(442) while for the CCWD case (442)>(311)>(111). This shows that copper chlorine introduces copper in the bulk of CdTe by changing its structure, affecting the orientation of the grains. Also AFM pictures show a slightly different grain structure, as depicted in figure 8.3.4.

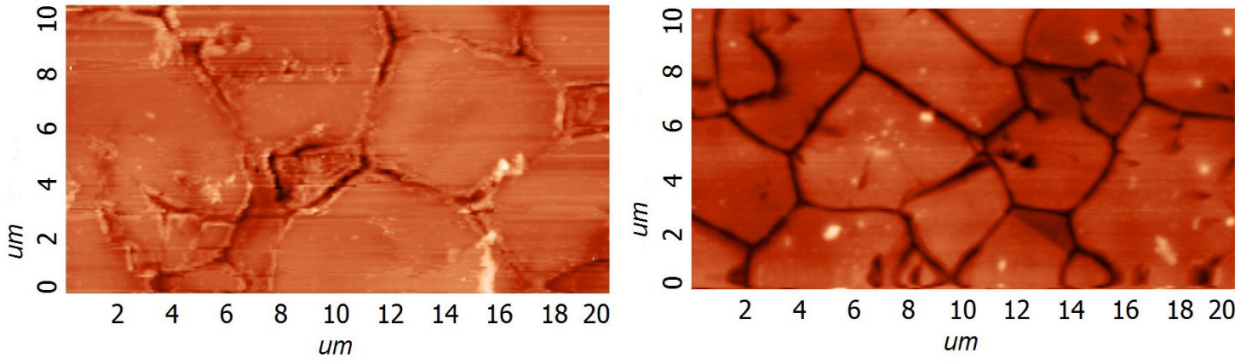

Figure 8.3.4. Morphology of CdTe before (left) and after (right) CCWD treatment process.

8.3.4 Doping and identification of defects

A very important aspect is understanding the effects of the different copper insertion processes in the CdTe doping. As already mentioned, a reduced Cu quantity would suggest a lower CdTe doping, but this appears to be in contrast with the devices performances, which in the case of CCWD samples does not suffer of any Cu deficiency. With capacitance voltage (CV) and drive level capacitance profiling (DLCP) measurements on VE-Cu and CCWD samples the net charge density in CdTe of acceptor-minus-donor states can be estimated as a

function of distance from the junction. The CV profiles (indicated in figure 8.3.5 with open dots) show the contribution of both deep and shallow defects, while the deepest states hardly affect the DLCP curves (full dots), so the difference between each pair of curves is associated to the presence of deep states [28].

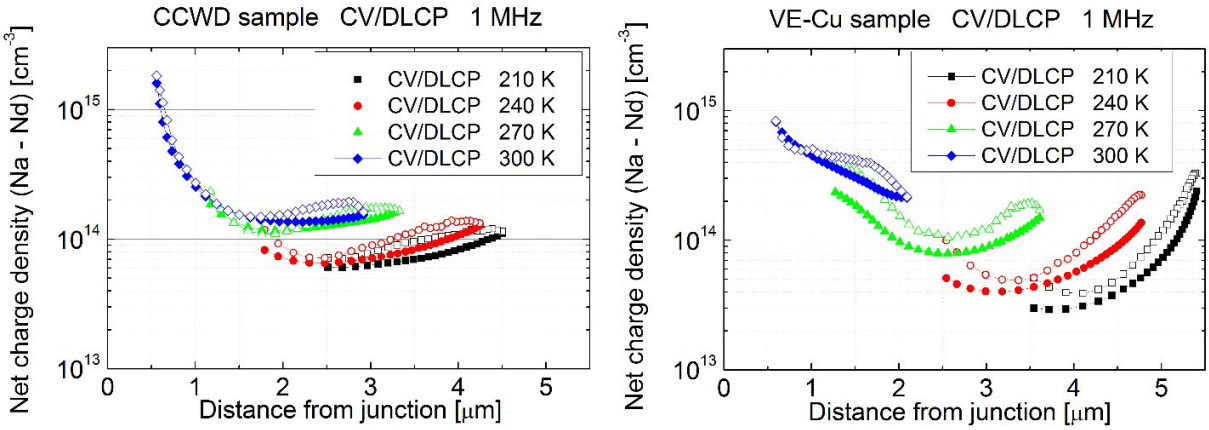

Figure 8.3.5: Comparison between CV (open dots) & DLCP (full dots) measurements of a CCWD sample (left) and a Cu sample (right) at 1 MHz.

At 1 MHz, the net charge density profile of the Cu sample (see figure 8.3.5, graph on the right) is much more temperature dependent than the $CuCl_2$ one: as the temperature rises, in the VE-Cu case (fig. 8.3.5, right side) the net charge density increases constantly with temperature, while in CCWD case (fig. 8.3.5 left side) the main increase happens only between 240 K and 270 K. This suggests that the dominant defects are of different nature in the two samples, however both kind of samples show the presence of deep defects. The net charge density is determined from the lower part of the U-shape profile in order to avoid effects due to others factors, such as a not perfectly ohmic back contact or the limited thickness of CdTe [29]. At 300 K the VE-Cu sample show a little higher net charge density than the CCWD case: 2 x10^{14} cm^{-3} versus 1.5 x 10^{14} cm^{-3}. At 210 K the net charge density of VE-Cu sample drops at 3 x 10^{13} cm^{-3} while it stays at 6 x 10^{14} cm^{-3} for the CCWD case, in the first case we can conclude that some defects freeze out. Again in figure 8.3.5, the profiles referred to the VE-Cu case increase in the right part of the graph; this effect is influenced by the back contact, revealing that the depletion region extends too close to the contact. Similar analysis has been done also at lower frequencies such as 10 kHz (see figure 8.3.6): in the VE-Cu case, we can imagine that some defects are slower and/or more distant from the valence band [30] compared to that of the CCWD case. The defects in the VE-Cu type are following the voltage signal at high temperature or at low frequency: so that at 10 kHz the net charge density is 3 * 10^{14} cm^{-3}. On the other hand for the CCWD sample the net charge density stays stable at 1.5 10^{14} cm^{-3}.

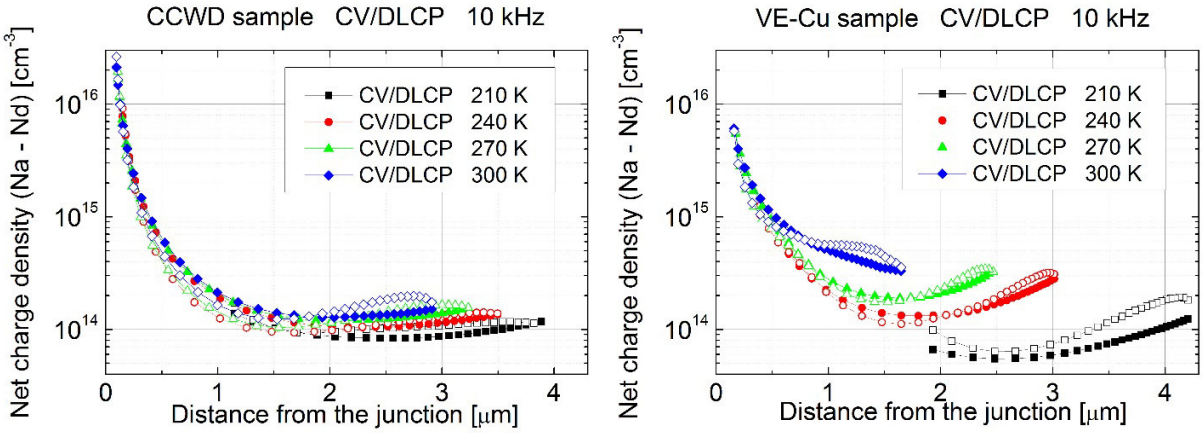

Figure 8.3.6. Comparison between CV (open dots) & DLCP (full dots) measurements of a CCWD sample (left) and a Cu sample (right) at 10 kHz.

Since the samples, except for the copper deposition step, have similar fabrication process, we can conclude that the $CuCl_2$ treatment gives place to different defects in the CdTe. However the overall net charge density is very close for the two processes. Thus it can be concluded that CdTe has similar level of doping with a reduced amount of Cu, if introduced with chlorine carrier, compared to the 2 nm thick copper layer deposited by evaporation. In order to identify the nature of the different defects seen by CV-DLCP measurements and to understand what happens when copper is introduced in CdTe bounded to chlorine, admittance spectroscopy analysis were performed on Cu and $CuCl_2$ samples. AS measurements allow to estimate the activation energy (E_a) and cross section (σ_a) of the dominant traps above the valence band and identify the nature of the defects (see figure 8.3.7 and table 8.3-III).

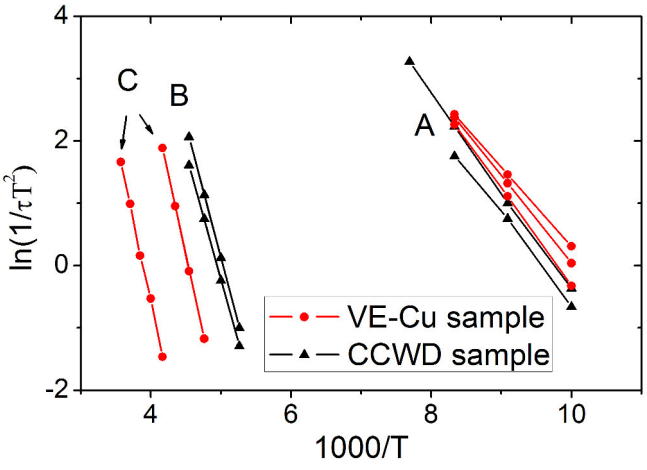

Figure 8.3.7. Arrhenius plot of the admittance spectroscopy data obtained from VE-Cu and CCWD samples.

Table 8.3-III: List of defects identified by admittance spectroscopy.

$CuCl_2$ sample		Attribution	Cu sample	
E_a [meV]	σ_a [cm^{-2}]		E_a [meV]	σ_a [cm^{-2}]
		A	109 ± 3	$1.9 * 10^{-16}$
125 ± 6	$4.6 * 10^{-16}$	A	121 ± 4	$5.5 * 10^{-16}$
136 ± 4	$2.0 * 10^{-15}$	A	134 ± 3	$1.7 * 10^{-15}$
349 ± 5	$2.0 * 10^{-13}$	B		
367 ± 6	$8.2 * 10^{-13}$	B		
		C	445 ± 10	$5.8 * 10^{-12}$
		C	449 ± 9	$1.9 * 10^{-13}$

Both samples show the presence of defect A, identified as the $V_{Cd} - Cl_{Te}$ complex, usually called A center [23]. However they show also different deep defects: in the $CuCl_2$ sample two defects (B) are detected: with E_a between 0.34 eV and 0.37 eV above the valence band, in this range the defects are attributed to the Cu at Cd substitutional sites impurities Cu^-_{Cd} [24,31]. These were also detected by Beach et al.: they reported that the concentration of these defects was higher in $CdCl_2$ treated samples, implying that the defects induced by $CdCl_2$ (probably Cl-induced donor) increased the solubility of Cu^-_{Cd} [24].
In this paper all the samples are $CdCl_2$ treated, however by detecting these defects only for the $CuCl_2$ sample suggests that Cl presence increases the Cu solubility into the CdTe bulk. Moreover, by reducing the amount of copper the number of interstitial copper defects Cu_i is also reduced.
It has been reported that the Cu substitution in Cd vacancy Cu^-_{Cd} acts as an acceptor, by increasing the p-type doping, while the interstitial copper Cu_i is a shallow donor, which compensate the doping [24,31,32]. For this reason the formation of the Cu^-_{Cd} defects is desirable.
On the other hand, Cu^-_{Cd} levels are not measured in the VE-Cu sample, despite the higher copper concentration. However this shows that this type of defect is not dominant in the VE-Cu sample. In this case, due to the large amount of copper, Cu^-_{Cd} and Cu_i are compensated. The VE-Cu sample shows two deeper dominant defects (C) in the range of 0.43 – 0.45 eV above the valence band, usually detected in our standard samples [16,33], which are not clearly attributed. Beach et al. [24] as well as Wei et al. [34] consider plausible to assign these values to the U-center Te^{2-}_i: a deep acceptor level. Also, Beach et al. highlight that these defects have a higher density for $CdCl_2$ treated samples, implying that $CdCl_2$ contributes to their formation, this has been previously observed also in our samples [33].

8.3.5 Analysis of the diffusion of copper element

Figure 8.3.8 shows HAADF images together with corresponding EDX Cu maps on $CuCl_2$ devices. In both samples, copper is distributed throughout the CdTe layer, including the back contact region. Nevertheless, in the picture it is clearly shown a larger uniformity of copper for the VE-Cu case (top), as a larger content of magenta colour is observable all over the CdTe bulk. On the other hand, the CCWD case shows a strong difference in the copper distribution: a higher contrast is observed near the back contact.

This suggests that in the $CuCl_2$ sample a larger amount of copper is fixed at the back contact despite it is 1/20 of the evaporated copper (see section 8.3.2). The fact that most of the copper introduced stays at the contact explains the lower back contact barrier in the $CuCl_2$ sample and so the high fill factor value.

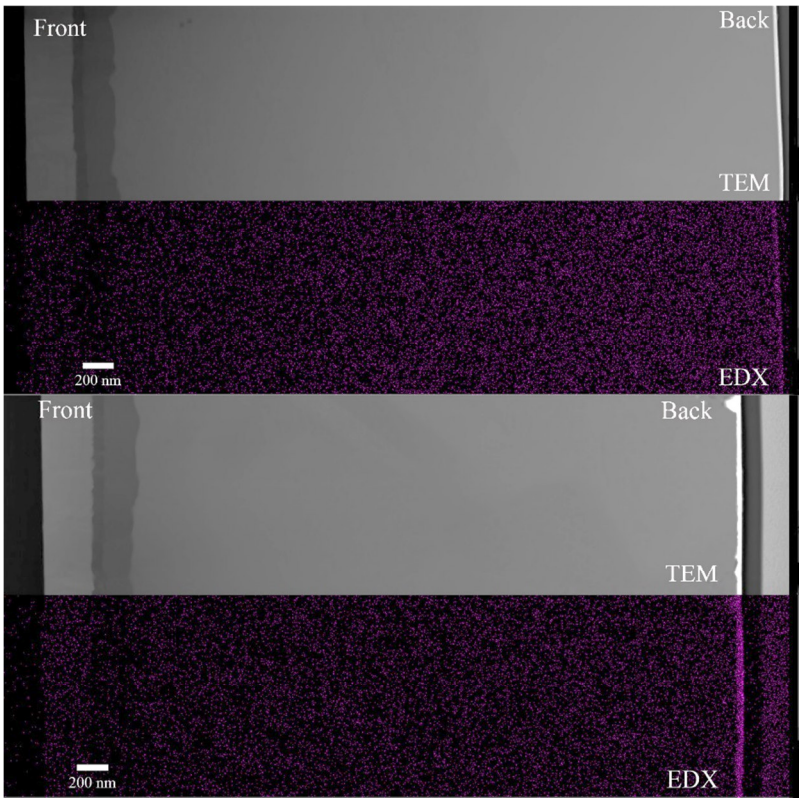

Figure 8.3.8: Comparison between HAADF images and corresponding EDX Cu maps of VE-Cu (top) and CCWD sample (bottom). While for the first case the magenta colour is almost homogeneously distributed for the second case it is concentrated at the back.

In order to check and confirm this observed different rate of copper diffusion, SIMS depth profiles have been analysed in the VE-Cu and the CCWD samples; both samples were coated with a 25 nm thick gold layer.
The SIMS profiles (shown in fig. 8.3.9) confirm the highest amount of copper on the surface for the VE-Cu case. Moreover in this sample there is a large copper diffusion in the first 400 nm (in depth), over this value the signal reduces at the limit of the sensitivity of the instrument. For the CCWD sample the signal decreases to the sensitivity limit within 200 nm; moreover the copper amount in this region is lower than in the VE-Cu sample. Finally, in the VE-Cu sample, we can observe copper diffusion inside the gold layer, due to the annealing of the finished back contact.

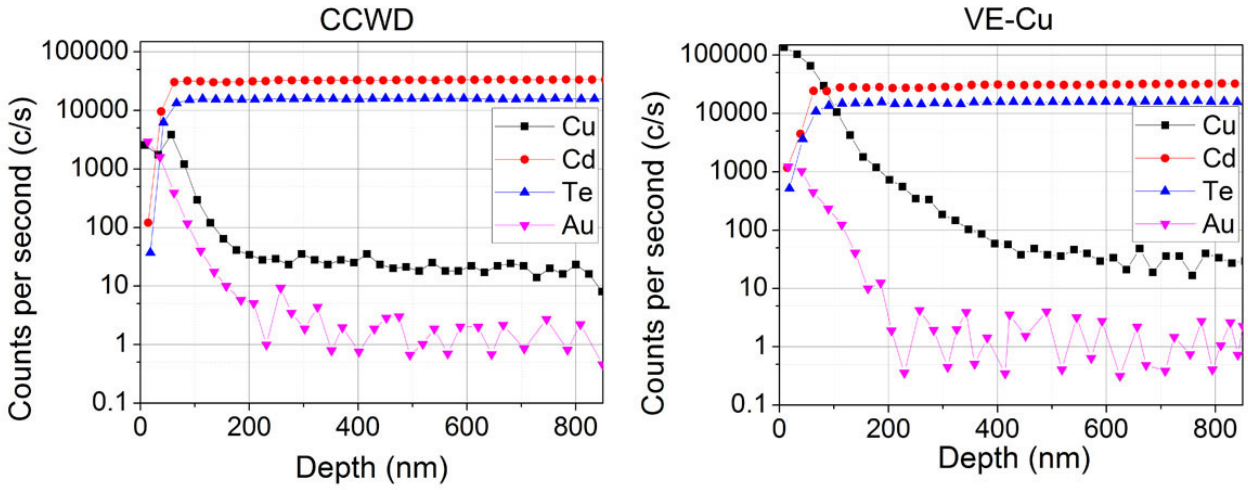

Figure 8.3.9: SIMS depth profiles of CCWD (left) and VE-Cu (right) finished devices.

8.3.6 Back surface analysis

Although the copper distribution in the CdTe varied dependent on the application method, it is useful to determine if it stays in elemental form or if it generates different compounds on the CdTe surface. For this purpose XPS characterization has been performed on the surface of VE-Cu and CCWD samples; both samples were prepared with only 5 nm thick gold layer on top, in order to allow the analysis.
In figure 8.3.10, the XPS Te 3d core levels show that while in the $CuCl_2$ sample Te-O and Te peaks have comparable heights, in the Cu sample the Te-O peaks are much more intense than the Te ones. Han et al. [35], reported a same increase of the Te-O peak and decrease of the Te peak when leaving the CdTe sample exposed to air. So we can conclude that in the VE-Cu sample the Te layer is mainly oxidized, while for the CCWD case Te-O and elemental Te have similar signals, thus the CCWD sample shows a larger presence of Te in the back contact region.

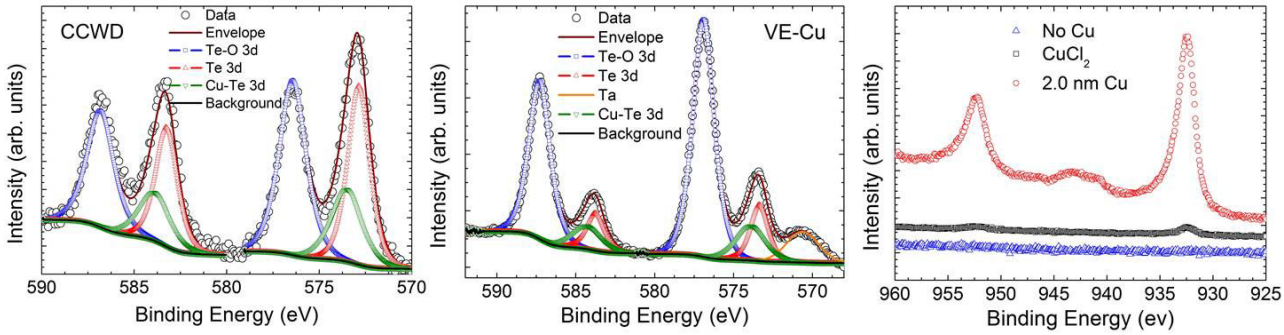

Figure 8.3.10: XPS spectra of finished CCWD (left) and VE-Cu devices (centre), and a comparison between the Cu peaks of the two devices (on the right) are shown.

This can explain the improved performance of the back contact for CCWD case (no rollover in the J-V curve is observed). A Te layer is widely used as a buffer to improve the back

contact because of its high valence band maximum, which is around 5.40-5.45 eV and stays at intermediate levels between the CdTe valence-band maximum (5.8 eV) below the vacuum level and the gold work function (5.1 eV). It reduces the CdTe back contact barrier [36].
Very important is that despite the lower Cu amount for the CCWD case, confirmed also by the XPS spectra (see figure 8.3.10, right), this sample shows high Cu-Te peaks. Thus in this case at the back contact it is placed a larger amount of copper (as supported by the already shown EDX mapping during TEM analysis).
From this analysis, we can conclude that depositing $CuCl_2$ on a Te rich layer (generated by the Br-MeOH etching), the Te binds with Cu during the annealing step oxidizing to a very limited extent. This is another part of the jigsaw that explains the higher performance of the back contact, since Cu_xTe buffer binds Cu and reduces its diffusion in the bulk as shown by Wu et al. [7]. This buffer can also be generated by depositing copper on the bromine-methanol etched CdTe surface as shown by Rimmaudo et al. [16].

8.3.7 Discussion and Performance stability of the cells

At this stage we have acquired that with a very minimum amount of copper it is possible to fabricate a performing back contact on the CdTe absorber layer if deposition is applied with $CuCl_2$. XPS, SIMS and EDX analyses confirm that a large amount of Cu is concentrated and fixed very near to the back contact suggesting a superior stability of the finished devices.
The best way to analyse and verify the performance degradation of the solar cells according to the different process discussed here, it is to apply accelerated stress tests (AST) on the photovoltaic devices. In a specific metal chamber, where a rack of halogen lamps and a temperature-controlled system allows to keep the cells under an illumination of one sun and at a temperature of 80°C, the cells are positioned for a time up to 1000 hours and their conversion efficiency measured every 300 hours.
Two different sets of solar cells were positioned in the AST box, one with VE-Cu samples and one with CCWD samples; both exhibited an average efficiency of about 14 % prior to aging. Their performance degradation has been analyzed by measuring their efficiencies at different time steps.

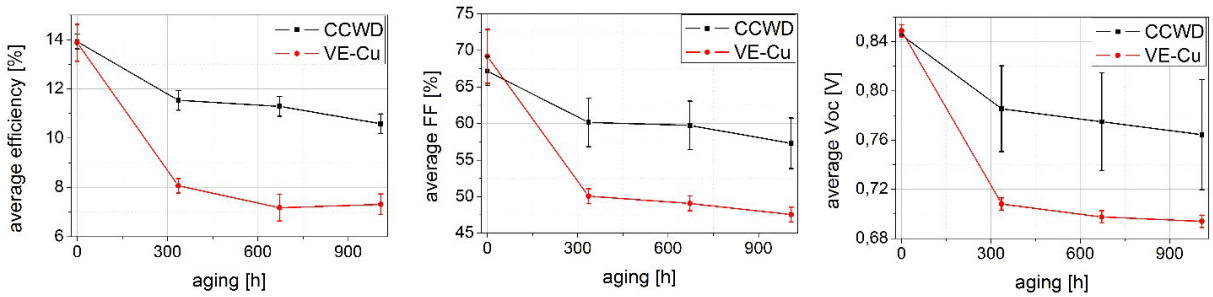

Figure 8.3.11: Graph reporting the performance degradation along time of the Cu and $CuCl_2$ samples. Results concerned to average efficiency on the left, to average FF in the center, and to average Voc on the right are respectively displayed.

Table 8.3-IV: average efficiency parameters of $CuCl_2$ and Cu devices before the aging, and after 1008 hours of AST.

Samples	η (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
$CuCl_2$ before aging	13.9 ± 0.3	67 ± 2	845 ± 3	24.5 ± 0.4
$CuCl_2$ after 1008 h of AST	10.6 ± 0.4	57 ± 3	764 ± 4	24.2 ± 0.4
Cu before aging	13.9 ± 0.8	69 ± 4	849 ± 5	23.6 ± 0.2
Cu after 1008 h of AST	7.3 ± 0.4	47 ± 2	694 ± 5	22 ± 1

As it can be seen in the graph on the left of figure 8.3.11 and on table 8.3-IV, the CCWD samples show a reduced degradation. In particular, after 1008 hours of aging they have an average efficiency of (10.6 ± 0.4) % compared to the (7.3 ± 0.4) % of the Cu samples. The cells show their major efficiency drop during the first period of aging, and also just after 336 hours the average efficiency discrepancy is clear: (11.5 ± 0.4) % versus (8.1 ± 0.3) %.
The different level of degradation depends mainly on the FF: after 1008 hours, setting to 100 the initial values, the average FF of CCWD samples is reduced to 85% of its initial value, the average Voc to 90%, and the average Jsc to 99%. On the contrary, the VE-Cu samples have reduced their average FF to 69%, their average Voc to 82%, and their average Jsc to 95%. After the complete AST cycle the CCWD samples exhibit 76% of the initial average conversion efficiency, while the efficiencies of the VE-Cu samples are halved.

The higher stability of CCWD-CdTe devices compared to the VE-Cu ones, as expected from the characterizations that have been discussed above, is confirmed. The extremely reduced amount of Cu (more than 20 times less) in the CCWD device also contributes to this stability. Diffusion is proportional to concentration, the amount of Cu which diffuses into the CdTe layer is regulated by its concentration gradient in the absorber film.
When large Cu amount is diffused, it can lead to shunt paths, reflecting in reduced FF as observed in this paper. So according to this argument, more Cu delivers increased migration towards the p-n junction. This hypothesis has been also partly confirmed by additional CV-DLCP characterizations, which were made on VE-Cu and CCWD samples after 336 h AST, where the main drop in efficiency value is occurred.
By comparing these profiles (shown in figure 8.3.12) with the pre-aging profiles depicted in figure 8.3.5, we can interpret the mechanisms of efficiency degradation. The net charge density of the CCWD sample drops from 1.5 x 10^{14} cm^{-3} to 5 x 10^{13} cm^{-3} after aging, and similarly the one of the VE-Cu sample, from 2 x 10^{14} cm^{-3} to 4 x 10^{13} cm^{-3}. More interesting, for VE-Cu case, the net charge density measured at lower temperatures (also shown in fig. 8.3.5) is low and the profiles are influenced by back contact effects (i.e. the depletion region extends too close to the back contact). As Cu increases, the extension of the depletion region widens to the metal back contact. This trend is stronger with time and can explain the reason of the larger reduction in performance of solar cells contacted with a 2.0 nm thick Cu layer.

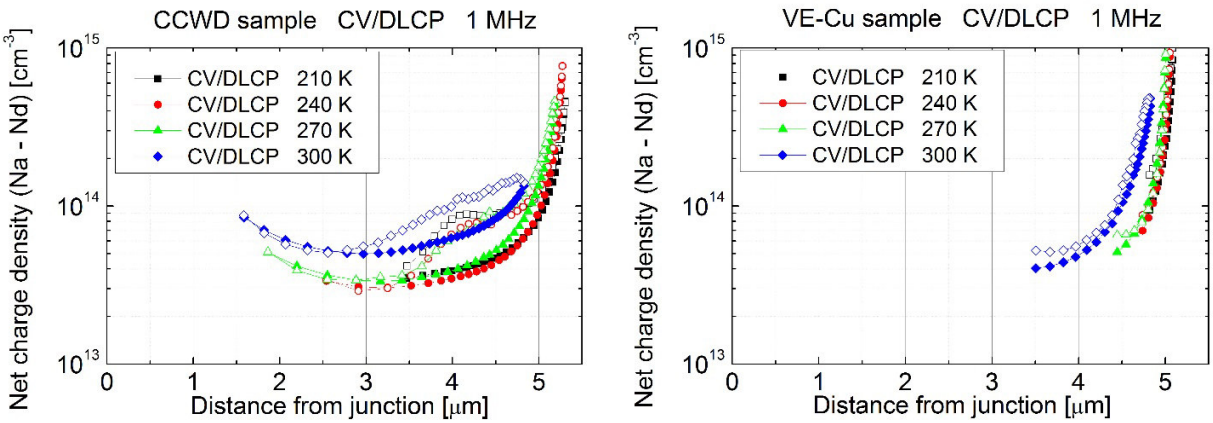

Figure 8.3.12: Comparison between CV (open dots) & DLCP (full dots) measurements of $CuCl_2$ sample (left) and Cu sample (right) after 336 hours AST.

A higher amount of copper diffusion from the back contact could lead to the formation of a larger amount of compensating defects. As also suggested by other groups, an excessive copper diffusion can compensate the Cu_{Cd}^- acceptors with Cu_i donors [6,32]. Therefore the smaller amount of Cu needed with the $CuCl_2$ copper deposition method leads to a reduced formation of compensating defects, and thus to the fabrication of more stable samples.

8.3.8 Conclusions

A wet deposition method has been developed in order to insert copper at the back contact of CdTe solar cells. Using a solution allows to simply deposit any ideal small amount of copper evenly over the entire area of the sample. In particular a copper chloride solution has been used because of the well-known effects of chlorine on CdTe such as recrystallization, grain growth [20], and possibly p-type doping [20,23].
The samples exhibit a good ohmic back contact without rollover and with efficiencies comparable to those of samples which are vacuum coated but with an amount of Cu twenty times larger. Moreover, a significant stability improvement has been achieved, as attested by the accelerated aging tests performed at an illumination of one sun and at a temperature of 80°C.
We have detected that the $CuCl_2$ treatment affects both bulk and back contact of the CdTe.

1. Bulk
CV-DLCP profiles of VE-Cu and CCWD samples reveal the presence of different dominant defects. Only for the CCWD sample the dominant defects, identified by AS, are in a range of energies that have been attributed to the substitutional Cu impurities Cu_{Cd}^- [24,31], known as acceptors in CdTe. Since all the different samples have been $CdCl_2$ treated, but only $CuCl_2$ treated samples show this type of traps, it can be supposed that the introduction of copper bounded to chlorine helps the solubility of the Cu_{Cd}^- acceptors since chlorine increases their solubility [24]. As a consequence, the p-type doping of CdTe is improved [6,36]. At low temperatures CV/DLCP show that VE-Cu samples are strongly influenced by back contact effects, their depletion region extends closer to the back contact, and thus the net charge

density is low. This effect appears mainly at the lowest temperatures, suggesting the presence of shallow donors, exactly as Cu_i, that, being closer to the band, have faster response at low temperatures than deep defects such as the Cu^-_{Cd} [30]. This effect increases with aging time, due to copper diffusion and consequent formation of Cu_i donors.

2. Back contact
Moreover, TEM images show for CCWD samples a larger inhomogeneity in copper distribution from the back contact to the junction, implying that the copper stays fixed at the back contact.
XPS spectra explain how the copper is fixed: in spite of the reducing copper quantity, the CCWD sample reveals a large presence of Cu-Te peaks, demonstrating that a Cu_xTe compound is formed stabilizing Cu at the back contact [7].
Compared to VE-Cu the CCWD process generates more elemental tellurium and less tellurium oxides, which is beneficial to the cell performance as Te layer is widely used as buffer to reduce the CdTe back contact barrier [36]. The improved back contact stability, given by the Cu-Te compounds, is supported by the reduced copper diffusion towards the CdTe/CdS junction; this has been confirmed by SIMS depth profiles.

Finally AST analysis has shown a different degradation of the solar cell devices according to the Cu inclusion method. For VE-Cu solar cells the degradation in performance is mainly due to the FF reduction. While for the CCWD cells, the degradation is very much limited.
In conclusion the $CuCl_2$ wet deposition process is a simple and advantageous method to insert copper in the back contact of CdTe solar cells. It allows the formation of Cu^-_{Cd} acceptor defects, reducing the formation of the compensating donors Cu_i.
In the light of the results obtained, the introduction of this method in the industrial production could really improve the lifetime of CdTe panels, without having too much efficiency losses.

8.3.9 References

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9
Final Conclusions

Polycrystalline thin film CdTe continues to be a leading material for the development of cost effective and reliable photovoltaics. Although research in CdTe dates back to the 1950s, it is a very innovative and promising technology. Thanks to the continuous development, in 2016 an efficiency of 22.1 % has been achieved, a gain of about 5 percentage point compared to the efficiency of 2012. In these last years many innovations have been made, but yet the theoretical efficiency has not been obtained and there is still a large room for improvement. Moreover many physical and electronic mechanisms in the devices are still not well understood, the understanding of which would lead to further improvement. Thus the research work on CdTe is far from being finished.
In our laboratory, superstrate configuration CdTe solar cells, fabricated by low temperature process, have achieved efficiencies exceeding 16 %. However, the continuation of our studies and the optimization of our processes will lead to even better efficiencies.
In this thesis I have presented the latest innovations we have introduced in the standard CdTe device: in particular our work and our studies concerning the window layer, the activation treatment, and the back contact. We did not just reproduce the changes introduced in the cells by the world leader First Solar; we looked for and followed different directions. Since it is very difficult to predict what direction will lead to the best results (as achieving the maximum theoretical efficiency and the improvement of the cells stability) it is very important to follow also alternative ways.

9.1 Study of alternative window/buffer layer

9.1.1 Ultra thin CdS window layer

Very thin CdS layers for CdTe solar cells have been prepared and treated in vacuum, argon and with a chlorine containing gas, at temperatures up to 550°C.
The treatment in difluorochloromethane gas (DFC-treatment) of a thin CdS layer, in the order of 30-80 nm, allows to improve the short circuit current of the devices, decreasing considerably the thickness of CdS, reducing the open circuit voltage loss. While, generally, cells with thin CdS layers are affected by micro-pinholes resulting in lower open circuit voltage.
Most probably the process protects the device from shunting, due to the larger grain size and the slight mix of CdS/ZnO layers.
Treatments at temperatures above 500 °C in argon and chlorine atmosphere on 80 nm thick CdS have led to the fabrication of more stable samples compared to not treated CdS, resulting in improved performance with a 10% increased current density and a 5% increased open circuit voltage and fill factor. Moreover, light transmission of the CdS treated layers from 300 to 450 nm is increased of about 10%.

9.1.2 MgZnO as HRT layer

The CdTe devices have been optimized for the introduction of a high resistance transparent layer of Mg-doped ZnO to replace our standard insulating ZnO layer. ITO/MZO layers were fabricated at Loughborough University with different substrate temperatures. The quantum efficiency measurement shows a different response according to the different TCOs: the insertion of the MZO layer improves the response across the entire wavelength range and in particular in the long wavelength region. This is not connected to a reduced absorption in the TCO and CdS layers. Cells with MZO deposited at temperatures above 300°C have resulted in a superior conversion efficiency compared to the standard process with ITO/ZnO solar cells. Different annealing temperatures of the $CdCl_2$ activation treatment have been applied to optimize the fabrication process. Most of the devices had superior efficiency, in the range of 14 % to 16 %. However, the best results were obtained by annealing the CdTe at 390 °C and by a reduction of the CdS thickness to 100nm. A FF improvement up to 74 % has been reached, which allowed to achieve efficiencies up to 16.2 %.

9.1.3 MgZnO window layer

Because of the tunable band gap of MZO, it is possible to tune the MZO band gap and electron affinity in a way to have an optimum match with CdTe, forming MZO/CdTe heterojunction. Thus we have fabricated CdTe solar cells by totally removing CdS and by using MZO as window layer. MZO was deposited in our laboratory by RF magnetron sputtering. The replacement of the CdS layer with the MZO dramatically increased the short circuit current. This has been confirmed by the EQE response, with a significant absorption improvement in short-wavelength region. On the other hand a slightly lower collection of photoelectrons in the 550-830 nm range compared to the sample with CdS has been recorded. This suggests a lower quality of the MZO/CdTe junction, which could be caused by the presence of a large amount of defects due to the reticular mismatch and possibly by an insufficient doping of MZO. This also explains the poor fill factor of the obtained samples. However good efficiencies close to 13 % have been obtained, with Voc above 885 mV and short-circuit current of 27.0 mA/cm^2.
We have obtained the best performances using a $Mg_{0,23}Zn_{0,77}O$ with a band gap of 3.72 eV. The band gap of the deposited MZO films range between 3.63 eV and 4.03 eV. In our deposition process the band gap is mainly influenced by the O_2 content in the RF-sputtering chamber rather than by the substrate temperature. Moreover, the magnesium content in the MZO film is also influenced by the amount of O_2 present in the chamber.

9.2 Study of the alternative $MgCl_2$ activation treatment

$MgCl_2$ has demonstrated to be a good alternative to the conventional $CdCl_2$ activation treatment, with the advantage to be non-toxic and less expensive. However devices produced with $CdCl_2$ still exhibit a higher efficiency. In our lab solar cells with efficiencies exceeding 14 % have been obtained by replacing the traditional treatment agent, $CdCl_2$, with $MgCl_2$. The samples have been characterized by CV and DLCP measurements, in order to obtain a

correlation between the treatment parameters and their effect on the electrical properties of the devices. Despite the similar shape of CV/DLCP spectra, at 300 K $CdCl_2$ treated devices exhibit a net charge density larger than any of the best samples processed with $MgCl_2$ treatment. At the same time, the $CdCl_2$ treated solar cells show a larger quantity of deep defects. AS measurements of the $MgCl_2$ samples show two deep defects that have been measured but not identified; only the best working devices did not exhibit these defects. These could be connected with Mg, since no similar ones have been detected previously for $CdCl_2$ treated devices. The other detected defects in the best $MgCl_2$ devices are very similar to those previously observed in the $CdCl_2$ case: mid gap defects, attributed to activation treatment, as well as Cu-related ones. Possibly a difference in their concentrations can justify the lower photovoltaic parameters of $MgCl_2$ solar cells.

9.3 Study of alternative back contact

9.3.1 MoO_x

Due to its high work function of about 6.8 eV, MoOx is one of the few semiconductors able to form an ohmic contact with p-type CdTe. For this reason a MoOx layer has been applied and optimized in order to produce a performing back contact without application of copper. MoOx has been deposited by reactive radio frequency sputtering of molybdenum in argon/oxygen atmosphere at room temperature. Finished devices have been fabricated with 20 % and 50 % oxygen/(argon + oxygen) ratio. With excessive amount of oxygen in the sputtering chamber, current density and therefore also efficiency are limited probably by a high back contact barrier. For this reason the CdTe cell fabrication process has been optimized by applying 20 % $O_2/(Ar+O_2)$ deposited MoOx. Moreover, solar cells have been grown with different thickness of MoOx. With a 9 nm thick layer the current voltage characteristic begins to show a marked roll over, for this reason our devices have been optimized with a 4-5 nm thick MoOx layer. The explanation can be attributed to the high resistivity of MoOx. Then devices with different copper thicknesses from 0.15 to 1 nm have been fabricated, in order to optimize the Cu quantity to dope CdTe avoiding shunts. Roll over is inversely proportional to the Cu amount, suggesting that, despite the MoOx insertion, copper strongly influences the ohmicity of the back contact. Moreover without copper the samples do not perform sufficient conversion efficiency. To avoid copper making contact in place of MoOx, the cells have been optimized by applying a 0.15 nm thick Cu layer. This process has led to the fabrication of samples with efficiencies exceeding 13%. However comparing cells contacted with and without MoOx followed by Mo, there are no significant differences in efficiency: cells with MoOx show an improved current, but also a larger roll over. This could be explained supposing that MoOx is blocking the carriers, since the electron affinity of the MoOx made by sputtering could be too low. Finally, in order to study the stability, cells contacted by MoOx/Mo and by Mo have been submitted to accelerated stability test (AST). These devices deteriorate faster than our standard cells. This could be related to the back contact degradation, thus to an instability of the MoOx layer. In conclusion MoOx deposited by reactive sputtering does not make a good ohmic contact with low substrate temperature CdTe. The insertion of MoOx improves neither the efficiency of our superstrate CdTe solar cells nor their stability.

9.3.2 Thin Cu layer

The doping and degradation mechanisms of Cu in CdTe solar cells are still not well understood, and for this reason they are an important topic. Doping is one of the major challenges of CdTe solar cells research, as it is the way to improve the open circuit voltage and attain even higher efficiencies. For this reason we have studied the influence of the thickness of the copper layer on the performances and on the degradation mechanisms of the devices. Reducing the thickness of the copper layer in the cells from 2.0 nm (our standard) to 0.1 nm, deposited by vacuum evaporation, the samples average efficiency decreases from 15.6 % to 13.3 %. Moreover this is obtained adding an annealing of the finished device at 300°C in air. The lower efficiency is caused by a marked roll over, symptom of a high back contact barrier. Thus, despite a very thin copper layer succeeds in CdTe doping, and despite CuTe compounds are detected from XPS measurements on CdTe surface even in the 0.1 nm sample, this thickness is not sufficient for a good contact ohmicity between CdTe and gold. However the analysis suggests that a 0.1 nm thick Cu layer is enough to dope a 7 μm thick CdTe layer, while the additional copper amount leads to the formation of compensating defects: a net charge density of an order of magnitude higher for the sample with the thin Cu layer, compared to our standard sample, is detected. Consistently, with DLTS we detect a single defect for the 0.1 nm case and two additional donor defects for the thick Cu case. AST show that samples containing a copper layer up to 0.5 nm thick are more stable in open circuit aging condition, while samples containing a 1.0-2.0 nm thick Cu layer are more stable in short circuit aging condition. A surprising inversion of the bias dependency happens between 0.5 and 1.0 nm, which is also the range in which the average efficiency increases from 13.5 % to 15.5 %. In samples with a thicker Cu layer, a higher amount of Cu diffusion from the back contact leads to the formation of a larger amount of compensating defects, as an excessive Cu diffusion can compensate the Cu_{Cd}^{-} acceptors with Cu_i donors. And it is well known, and it has been widely experimented, that copper diffusion is favored in open circuit condition. On the other hand, in samples with a thinner Cu layer, another degradation mechanism predominates. In this case the net charge density decrease could be associated with the decay of the Cu_{Cd} acceptor into the donor acceptor pair Cu_i V_{Cd}. This phenomenon is probably enhanced by the current flow present in the sample in the short circuit condition, moreover the poor presence of interstitial copper and of copper diffusion from the contact makes the formation of others Cu_{Cd} states unlikely.

9.3.3 $CuCl_2$ treatment

An innovative $CuCl_2$ wet deposition method has been developed. This process allows reduction of the incorporated copper quantity without any loss in performance compared to a standard Cu contacting route and simple and rapid depositing evenly over the entire area of the sample. In fact, the $CuCl_2$ samples exhibits a good ohmic back contact without rollover and with efficiencies comparable to those of samples which are vacuum coated but with an amount of Cu twenty times larger. We have detected that the $CuCl_2$ treatment affects both bulk and back contact of the CdTe.
The comparison of CV-DLCP profiles of $CuCl_2$ processed samples with our standard ones reveal the presence of different dominant defects. Only for the $CuCl_2$ samples the dominant defects, identified by admittance spectroscopy measurements, are in a range of energies that

have been attributed to the substitutional Cu impurities Cu^{-}_{Cd}, known as acceptors in CdTe. Thus the introduction of copper bounded to chlorine helps the solubility of the Cu^{-}_{Cd} acceptors, reducing the formation of the compensating donors Cu_i, improving the p-type doping of CdTe.
Compared to our standard sample, TEM images show for the $CuCl_2$ sample that copper stays fixed at the back contact. XPS spectra reveal, for $CuCl_2$ sample, a large presence of Cu_xTe compounds. Furthermore, the $CuCl_2$ treatment generates more elemental tellurium, which also reduces the CdTe back contact barrier. SIMS profiles show, for the $CuCl_2$ sample, a reduced Cu diffusion into CdTe bulk and thus towards the CdTe/CdS junction, confirming an improved back contact stability.
$CuCl_2$ treated devices show a dramatic improvement in performance stability: after 1000 hours of AST they exhibit 76 % of the initial average conversion efficiency, while the efficiencies of the standard samples are halved.
In the light of the results obtained, the introduction of this method in the industrial production could really improve the lifetime of CdTe panels, without having efficiency losses.

List of publications

1) E. Artegiani, D. Menossi, H. Shiel, T. D. Veal, J. D. Major, A. Gasparotto, K. Sun, and A. Romeo, "Analysis of a novel $CuCl_2$ back contact process for improved stability in CdTe solar cells", submitted for publication.

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Audentis fortuna iuvat
(Virgilio, Eneide X, 284)