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Paper

An Innovative Approach to Multi-Valued Logic

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The current generation of computer systems operates on the principles of binary logic, which encompasses both logical and arithmetic operations. However, silicon technology has reached its peak performance, prompting researchers to explore alternative methods for enhancing computational efficiency. One such method is the adoption of Multi-Valued Logic (MVL) technology, which offers a promising avenue for increased computational efficiency. This study introduces a novel decenary logic family, implemented using analog circuitry with significantly reduced complexity. The proposed circuits are designed in both analog and voltage modes. Designing Min, Max, Optimism Step (OS), and Pessimism Step (PS) operators a universal logic family is introduced. Finally, experimental results were presented and compared against various binary and MVL technologies. These circuits are proof of concept and can be implemented using new technologies such as GaN to significantly reduce the size of transistors. © 2026 The Author(s). *IEEJ Transactions on Electrical and Electronic Engineering* published by Institute of Electrical Engineers of Japan and Wiley Periodicals LLC.

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1. Introduction

Binary systems have reached their limit. Multi-valued logic (MVL) can be a potential solution to overcome the limitations of binary logic [1]. Analogous to the binary logic family, the MVL family encompasses two types of circuitries: logical circuits and arithmetic circuits. The adoption of MVL-based computational technology enhances processing power, data transfer rate, and data storage capacity compared to the current binary technology. The use of MVL not only improves processing performance but also decreases the required clock rate for the processor. MVL technology offers greater processing power with fewer transistors and reduced power consumption, where a lower clock rate further diminishes the power consumption of MVL-based devices.

Researchers have implemented MVL circuits using different technologies. Carbon nanotube field-effect transistor (CNTFET) with adjustable threshold voltages is one of the technologies used to implement MVL circuits. Ability to create different voltage levels through adjustable threshold voltages makes CNTFETs an interesting approach in MVL circuit design [2–9].

In a reported work by Hosseini *et al.* a novel ternary and quaternary MVL comparator was introduced [10]. The multi-threshold voltage CNTFET is the main element used in developing this comparator. The reported comparator is designed and simulated in both ternary and quaternary modes. The interesting feature of this design is claimed to be the possibility of extending the ternary function into a quaternary function using only four additional transistors. This design is simulated using Stanford 32 nm CNTFET library in HSPICE. In a reported work by Soliman *et al.* [11], a two-bit ternary adder and multiplier is presented. The proposed designs are verified using VTEAM memristor and Stanford CNTFET transistor models. The authors claim that the proposed design increases performance, reduces the number of transistors, and lowers power consumption compared to the reported related works; however, no comparison was reported. In reported work with Haq *et al.* [12], the authors present a low-power quaternary logic design combining CNTFETs and RRAM. Using a 32 nm model at 0.9 V, the proposed gates and arithmetic circuits (inverter, NAND, NOR, half adder, multiplier) achieve up to 93% lower PDP than prior designs. The hybrid approach provides non-volatility, single-supply operation, and high PVT stability, making it suitable for energy-efficient and reconfigurable computing.

Fakhari *et al.* [13] reported a new quaternary adder based on CNTFET switching logic. The proposed circuit was simulated in HSPICE using the Stanford CNTFET model. A layout for the MVL full adder was reported in this work.

In another reported work by Haq *et al.* [14], they propose a 1-trit ternary multiplier using graphene nanoribbon FETs (GNRFETs) with only 26 transistors. Simulations at 32 nm and 0.9 V show 21.4% lower delay, 33.1% lower PDP, and 58.2% lower EDP than prior designs. The circuit uses a single power supply, avoids direct VDD–ground paths, and remains stable under PVT and load variations, making it ideal for low-power portable systems.

Another interesting technology used in building MVL circuits is the Single-Electron Transistor (SET) which offers very low energy consumption [15,16]. For instance, in a work reported by Fresch *et al.* [17], two different physical systems were used for multivalued calculation. The first reported system is called molecular system with parallelism as its main feature. Fresch *et al.* [17] expressed their concern about numerous problems associated with using single-electron systems. Lithography of single electron

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systems requires $E_c \sim 100K_BT$ technology which is difficult to implement in VLSI. Controlling randomness of the background charges is also a major challenge in using single-electron systems.

The Quantum-dot Cellular Automata (QCA) is yet another popular technology with close to zero power consumption. This technology operates through electric field interactions between cells. There is no electric current in QCA; this is due to the fact that electrons are confined within a square and can only move within this square without consuming any power [18,19]. Mohaghegh *et al.* [20] used QCA as a tool to develop a Ternary QCA (TQCA)-based full adder. Mohaghegh *et al.* simulated their design using TQCASIM software.

Charjee *et al.* [21] report a novel Random Access Memory (RAM) using MVL and fuzzy logic operators. Authors used a fuzzy interface system with a limited number of logical steps and a 1×3 memristive crossbar array to develop an MVL-based RAM (MVLRAM). Chawdhury *et al.* [22] reported Max and NOR operators in voltage mode. The Max operator uses only three transistors. Adding two more transistors, this operator converts to a NOR operator. Chawdhury *et al.* simulated their design in HSPICE using an 180 nm library. Vasundara Patel *et al.* [23] presented arithmetic operations such as addition and multiplication in modulo-4 arithmetic. They have also reported addition and multiplication operators in Galois logic using MVL [23]. Vasundara Patel *et al.* [23] reported a quaternary convertor to convert from binary to quaternary and back. The authors have not reported a designed circuit at the transistor level in their paper, and they only reported a block diagram for the design. Okihiko Ishizuka *et al.* [24] presented an algorithm for MVL multiplication with an MVL redundant adder. The authors reported a current-mode circuit design and design layout for 4×4 and 16×16 quaternary multipliers. The proposed design suffers from current limitation problems such as fan-out and static power usage. Researchers are working on modern technologies applicable to the MVL research area. For instance Karmakar [25], presented QDG-SWSFET, which is a combination of Quantum Dot Gate FET and Spatial Wave-function Switch FET. Karmakar [25] provided a quaternary inverter gate. The inverter gate operates using a single 3 V power supply.

There are a limited number of reports that utilize MOSFET, for instance the work reported by Wang *et al.* [26]. This work presents a study on balanced ternary digital logic circuits using memristors and NMOS technology, highlighting their differences from traditional binary circuits. It details the design of basic balanced ternary gates, including TMIN and TMAX, as well as encoders, decoders, and combinational logic circuits like half-adders and multipliers. The reported circuits were simulated using LTSpice and validated through experiments with fabricated memristors, demonstrating effective performance. A comparison of decoder-based and multiplexer-based design methods revealed advantages in component count and power consumption for the former. Findings suggest that these ternary circuits can enhance efficiency and density in digital logic applications. Overall, the reported research contributes to the development of advanced computing architectures beyond traditional binary systems.

In another paper presented by Zhao *et al.* [27], advancements in ternary logic circuits are reported emphasizing their potential for higher data density and lower power consumption in comparison to the binary systems. Zhao *et al.* [27] introduce optimized ternary arithmetic circuits, including adders and multipliers, designed with ternary cycling gates to enhance efficiency and reduce circuit complexity. The proposed ternary full adder achieves a power-delay product (PDP) of 11 aJ at 0.5GHz, marking a significant improvement compared to previous designs. Additionally, the implementation of high-speed ternary Wallace tree multipliers demonstrates an average PDP improvement of 36.8% in comparison to classical designs. The successful application of these methods using standard CMOS technology indicates a promising future for ternary computing in practical electronics.

The current paper is organized into 11 chapters. Chapter 1 provides an introduction and discusses related work in this area. Chapter 2 outlines the problem definition and explains the proposed method of approach. Chapter 3 introduces the proposed algebraic logic family. Chapter 4 presents circuit specifications for the proposed design. Chapter 5 introduces the early circuit design, called the Analog Buffer, that increases fan-out of the proposed logic's circuitry. Chapter 6 introduces the Max operator, and Chapter 7 the Min operator. In Chapter 8, applying Optimism Step (OS) and Pessimism Step (PS) operators, the decenary MVL introduced in earlier chapters is extended to universal logic. Chapter 9 provides a comparison between the proposed MVL family circuit and several different technologies. Chapter 10 concludes the paper, and Chapter 11 discusses future work.

2. Problem Definition

As discussed in the introduction, MVL-based technology holds significant potential benefits. A group of researchers is actively engaged in this field, leading to the introduction of modern designs and logic families.

This article presents a novel MVL-based logic family. The ultimate objective of the project is to design components for a decenary Arithmetic and Logic Unit (ALU) and memory. The reported work focuses on the logic unit of a decenary ALU, which necessitates a decenary logic family.

The reported work introduces four logical operators Min, Max, OS, and PS to meet the criteria for defining a universal logic family. These operators are inherently analog and designed to operate in an analog mode. However, they can function in either analog or digital modes based on their inputs, accommodating both continuous values and quantized levels. Most MVL research is based on emerging technologies, which often face the challenge of limited commercial availability.

Utilizing commercial parts is appealing but comes with its own set of problems, such as dealing with nm-scaled transistors that have low breakdown voltages, static threshold voltages, and a limited variety of electronic components at the nm scale. In this work, 180 nm technology was employed to address issues related to the breakdown voltage of 180 nm-scale transistors.

The authors opted for analog mode in the design of logical operators to circumvent the limitations of switching designs. Analog circuit design facilitates the creation of low-complexity circuits using one or two power supplies. While analog design offers advantages, it also has drawbacks, such as higher static power consumption and greater sensitivity to noise compared to digital design. MVL circuits operate at quantized levels, and the proposed logic family operates in quantized mode with quantized inputs.

This paper introduces five distinct circuits. The first circuit is the Analog-buffer (A-buffer), which serves as an output driver and is present at the output of all operators in the proposed logic family to enhance fan-out. The second circuit is the Max operator, which operates in three stages and includes an A-buffer at its

output (Stage 3). The third circuit is the Min operator, like the Max operator in its three-stage operation and an A-buffer at its output (Stage 3). Sections V and VI explain the Min and the Max operators. It is important to note that the proposed logic family is not universal without the additional OS and PS operators, that is, it cannot implement arbitrary logic functions. Hence, to achieve universality, two additional operators, OS and PS, are introduced.

3. Proposed Decenary MVL Family

Surveying related work in this area showed that existing studies are primarily focused on single operators in n-ary MVL or on the implementation of binary logic components within MVL frameworks. To the best of our knowledge, there are no reported works on the introduction of a complete solution in the form of a hardware-implemented MVL family that satisfies algebraic models. A hardware implementation of an MVL family must be supported by algebraic theories and axioms to be considered valid. This section describes the proposed Decenary-MVL (D-MVL) family using the algebraic model of the proposed operators. Equation (1) defines the proposed algebraic system.

$$(\boldsymbol{D}; \oplus, \odot, \uparrow, \downarrow) \tag{1}$$

To establish a theoretical foundation for the proposed D-MVL family, algebraic concepts such as domain and board are applied to the D-MVL family. Equation (2) defines the members of the decenary D set.

$$\boldsymbol{D} = \{0, 1, 2, 3, 4, 5, 6, 7, 8, 9\} \tag{2}$$

The operators within the proposed D-MVL family are defined in (3) through (6).

$$\oplus = MAX\ operator \tag{3}$$

$$\odot = MIN\ operator \tag{4}$$

$$\uparrow = O.S\ operator \tag{5}$$

$$\downarrow = P.S\ operator \tag{6}$$

Initially, ring axioms for the D-MVL family are introduced, and some proofs are provided. Extending the ring axioms, domain axioms are introduced to the D-MVL family to complete the algebraic support for the D-MVL family. To constitute a ring, seven axioms must be satisfied, as outlined in (7) through (13) [28–30].

Associative

$$\forall \alpha, \beta, \gamma \in \mathbf{D}, \alpha \oplus (\beta \oplus \gamma) = (\alpha \oplus \beta) \oplus \gamma \tag{7}$$

$$\forall \alpha, \beta, \gamma \in \mathbf{D}, \alpha \odot (\beta \odot \gamma) = (\alpha \odot \beta) \odot \gamma \tag{8}$$

Identity

$$\exists 0 \in \boldsymbol{D} \mid \forall \alpha \in \boldsymbol{D}, 0 \oplus \alpha = \alpha \oplus 0 = \alpha \tag{9}$$

Inverses

$$\forall \alpha \in \boldsymbol{D}, \exists (-\alpha) \in \boldsymbol{D} \mid \alpha \odot (-\alpha) = (-\alpha) \odot \alpha = 0 \tag{10}$$

Commutative

$$\forall \alpha, \beta \in \mathbf{D}, \alpha \oplus \beta = \beta \oplus \alpha \tag{11}$$

$$\forall \alpha, \beta \in \boldsymbol{D}, \alpha \odot \beta = \beta \odot \alpha \tag{12}$$

Distributive law

$$\forall \alpha, \beta, \gamma \in \mathbf{D}, \alpha \odot (\beta \oplus \gamma) = (\alpha \odot \beta) \oplus (\alpha \odot \gamma) \tag{13}$$

The D-MVL family is called a field if defined within the D set by replacing the Max operator with the addition operator and the Min operator with the multiplication operator, respectively. The proposed algebraic system adheres to the field axioms. By assigning all domain values to all the elements within the axiomatic fields, it was proven that all 10 axioms are correct within (D; $\oplus$, $\odot$, $\uparrow$, $\downarrow$). Consequently, (D; $\oplus$, $\odot$, $\uparrow$, $\downarrow$) constitutes a field. The field axioms of the proposed system are defined in (14) through (24) [28–30].

The inverse axioms and their corresponding $-\alpha$ and $1/\alpha$ values are defined in (25) and (26).

Closure.

$$\forall \alpha, \beta \in \mathbf{D} \mid \alpha \oplus \beta \in D \tag{14}$$

$$\forall \alpha, \beta \in \mathbf{D} \mid \alpha \odot \beta \in D \tag{15}$$

Commutative

$$\forall \alpha, \beta \in \mathbf{D}, \alpha \oplus \beta = \beta \oplus \alpha \tag{16}$$

$$\forall \alpha, \beta \in \mathbf{D}, \alpha \odot \beta = \beta \odot \alpha \tag{17}$$

Associative

$$\forall \alpha, \beta, \gamma \in \mathbf{D}, \alpha \oplus (\beta \oplus \gamma) = (\alpha \oplus \beta) \oplus \gamma \tag{18}$$

$$\forall \alpha, \beta, \gamma \in \mathbf{D}, \alpha \odot (\beta \odot \gamma) = (\alpha \odot \beta) \odot \gamma \tag{19}$$

Identity

$$\exists 0 \in \mathbf{D} \mid \forall \alpha \in \mathbf{D}, 0 \oplus \alpha = \alpha \oplus 0 = \alpha \tag{20}$$

$$\exists 9 \in \mathbf{D} \mid \forall \alpha \in \mathbf{D}, 9 \odot \alpha = \alpha \odot 9 = \alpha \tag{21}$$

Inverses

$$\forall \alpha \in \mathbf{D}, \exists (-\alpha) \in \mathbf{D} \mid \alpha \odot (-\alpha) = (-\alpha) \odot \alpha = 0 \tag{22}$$

$$\forall \alpha \in \mathbf{D}, \exists (1/\alpha) \in \mathbf{D} \mid \alpha \oplus (1/\alpha) = (1/\alpha) \oplus \alpha = 9 \tag{23}$$

Distributive law

$$\forall \alpha, \beta, \gamma \in \mathbf{D}, \alpha \odot (\beta \oplus \gamma) = (\alpha \odot \beta) \oplus (\alpha \odot \gamma) \tag{24}$$

4. Circuit Specifications

Power supply voltage and number of logical levels are critical parameters in the design of MVL circuits. The power supply voltage is constrained by the breakdown voltage of the technology employed in the design. For instance, the typical breakdown voltage for 130 nm scale MOSFET transistors begins at approximately 5.5 V [31].

In the reported work, Taiwan Semiconductor Manufacturing Company (TSMC) 180 nm technology, with its specified 5.5 V power supply voltage selected for implementation. The threshold voltage for TSMC 180 nm technology is approximately 0.5 V. Consequently, the voltage difference between the two levels in the proposed Differential MVL (D-MVL) logic family is set to 0.5 V, which corresponds to the noise immunity. Although these operators function in analog mode, they can operate within other voltage differences as well. In the D-MVL system, power supply

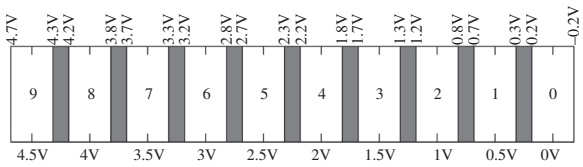

Fig. 1. Valued and undefined regions

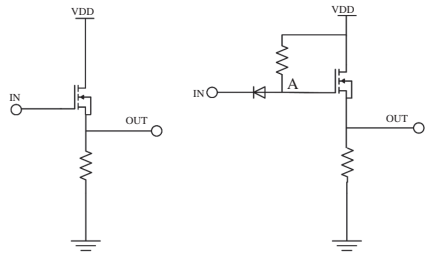

Fig. 2. Analog Buffer

voltage restricts the number of the levels and the distance between them. Figure 1 illustrates the voltage levels, their corresponding logic values, and the undefined regions in the proposed D-MVL system.

$$\forall \alpha \in \mathbf{D} : -\alpha = 1 \downarrow \alpha \tag{25}$$

$$\forall \alpha \in \mathbf{D} : 1/\alpha = 9 \downarrow \alpha \tag{26}$$

5. A-Buffer

A-buffer is an analog buffer designed in two parts, as depicted in Fig. 2. To provide a better understanding, A-buffer was initially designed using discrete components. Part 1 of the circuit represents the A-buffer's output circuit. Figure 2(a) illustrates the output stage of circuitry. Functionality of the A-buffer is explained in detail in Equation (27).

$$V_{out} = V_i - V_{th} \tag{27}$$

Where V_{th} is the threshold voltage of an N-channel MOSFET. Part 2 includes a resistor functioning as a pull-up circuit and a diode to increase the input voltage. By pulling-up the input voltage, voltage at point A in Fig. 2(b), will be $V_{in} + V_{th}$ and consequently, the output voltage will be equal to $(V_{in} + V_{th}) - V_{th} = V_{in}$. Figure 3 shows three different parts of design, i.e. resistor model, diode model and TSMC 180 nm integrated A-buffer circuit. These circuits were simulated using PSPICE. Figure 4 shows the simulation results.

5.1. TSMC 180 nm buffer Figure 2(b) shows design of an A-buffer using TSMC 180 nm technology, wherein diodes and resistors were modeled using 180 nm MOSFET transistors. A transistor biased using the calculated threshold voltage can replace a resistor. It is also common knowledge that NMOS transistors can model a diode once their gate is connected to their drain [32]. As depicted in Fig. 2(b), the input of the circuit needs to sink current from VDD to the input to keep the diode on. This implies that, like TTL, there is a current fan-in for each circuit input. To address A-buffer's fan-in problem, an additional transistor was

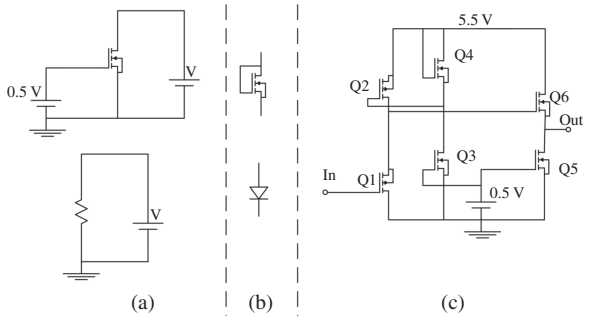

Fig. 3. Proposed component models (a) Resistor model (b) Diode model (c) TSMC 180 nm buffer

added to the new design, freeing the input from requiring a driving current for its operation (Fig. 3(c)). In Fig. 3(c) Q2, Q3, and Q5 function as resistors, Q4 works as a diode, Q1 is pulling down the input, and Q6 is pulling up the output. Figure 4 shows the simulation results. The proposed circuit can operate in both analog and MVL modes, whether the input signal is continuous or quantized. The A-buffer simulation results are reported using four distinct types of input signals, i.e., analog, binary, seven-valued MVL, and decenary MVL.

6. Max Operator

Max operation is the same as logical OR in binary circuits. In other words, OR gate in binary logic is the same as the Max operator. Initially, the Max operator was introduced using discrete elements. Figure 5 illustrates the Max operator in a discrete circuit design. Figure 6 shows a Max operator designed using a 180 nm scaled integrated circuit.

In Fig. 5, the value of resistor R1 must be much smaller than that of resistor R3. Only one of the inputs, IN1 or IN2, with the highest voltage can turn on its associated diode, either D1 or D2. Diodes D3 and D4 are used as voltage shifters to compensate for the threshold voltages of diodes D1 or D2 and the threshold voltage of transistor Q1. The output stage of the Max operator works similarly to the output stage of the A-buffer. The output voltage is calculated using (28).

Let us assume that diode and transistor threshold voltages are the same. D3 and D4 threshold voltages were used to compensate for threshold voltages of input diodes and Q1 transistor.

TSMC180 nm Max operator.

Figure 6 shows Max operator designed using TSMC 180 nm technology. The Max operator is structured in three stages as follows.

1. Input stage (Q1, Q2, Q3, Q4)
2. Middle stage (Q5, Q6, Q7, Q8, Q9, Q10)
3. Output stage (Q11, Q12, Q13, Q14)

Transistors Q3 and Q4 function as pull-down resistors. Transistors Q1 and Q2 operate with high impedance inputs. In the intermediate stage, Q9 and Q10 integrate signals and elevate the input voltage by one level, specifically by 0.5 V.

$$V = Max(V_{in1}, V_{in2}) - V_{th} \tag{28}$$

The output stage reduces the voltage level by one using a PS operator. The architecture of this stage is akin to the output

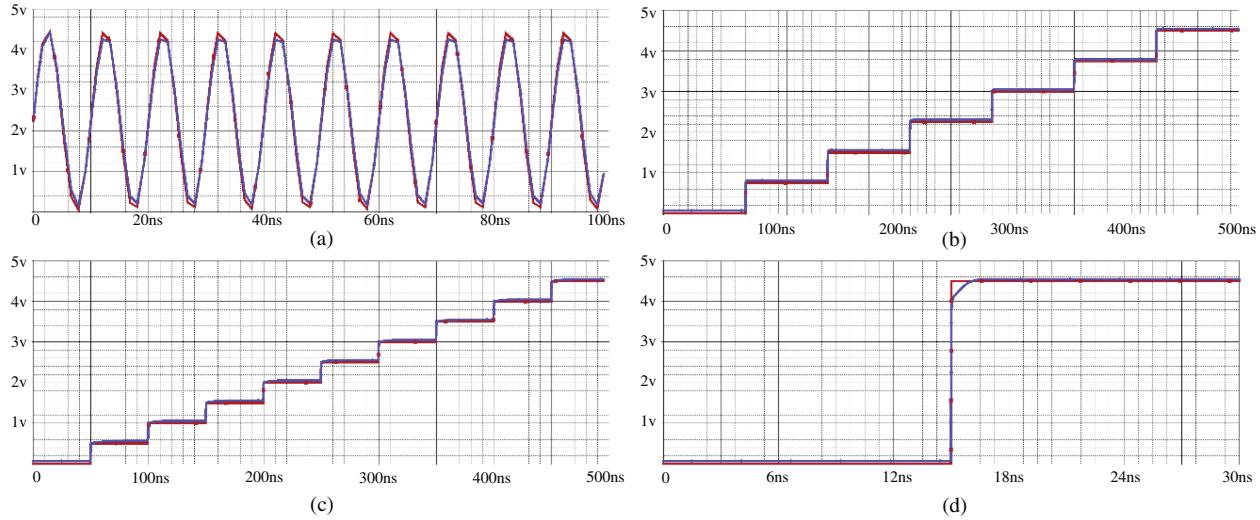

Fig. 4. Buffer 180 nm simulation (a) Analog input/output (b) Seven valued (c) Ten valued (d) Binary input/output (input is in Red, output is in Blue)

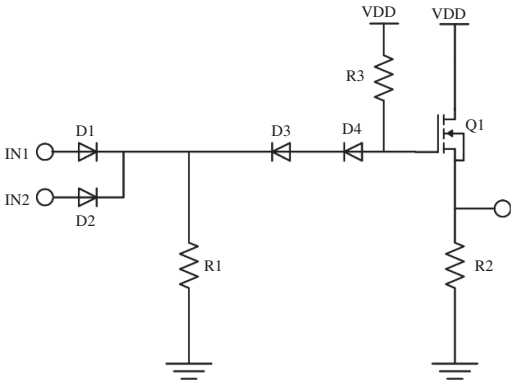

Fig. 5. Discrete circuit implementation of the Max operator

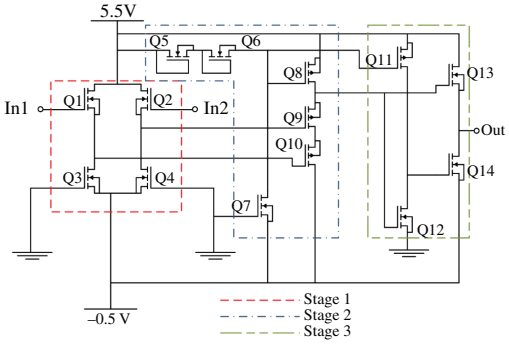

Fig. 6. Max operator in TSMC 180 nm

stage of an A-buffer, with the addition of a variable pull-down impedance. Max operator circuit is simulated using PSPICE, with the simulation results presented in Fig. 7. These simulations encompass four distinct input models for the Max operator: binary inputs, seven-valued logic, decenary logic, and a sinusoidal signal. The proposed Max operator circuit design consists of 14 transistors. Spikes are observed at the output during the rising edges of the input level changes. The occurrence of these spikes is documented in Fig. 7(a)–(c). Design of a 10-valued quantized buffer in 180 nm technology is already reported [33]. Three axioms of the algebraic field are demonstrated in Fig. 7: Closure, Commutativity, and Identity. In switching logic mode design, two significant challenges arise: firstly, the number of transistors increases with the number of levels; secondly, the circuit is limited to operation within a predetermined number of levels. In analog-based logic circuitry, there is no distinction between an n-level logic circuit and an $(n+1)$-level logic circuit.

7. Min Operator

Min operator functions as a logical AND in binary circuits. Figure 8 illustrates the discrete Min operator.

The discrete Min operator is identical to the discrete A-buffer, with the addition of one more diode in its input stage. Diodes D1 and D2 serve as minimum voltage finders for the In1 and In2 inputs.

TSMC 180 nm Min operator.

The Min operator, like the Max operator, consists of three stages. This structure is illustrated in Fig. 9.

- Input stage (Q1, Q2, Q3, Q4, Q5, Q6)
- Middle stage (Q7, Q8, Q9)
- Output stage (Q10, Q11, Q12, Q13)

Transistors Q3 and Q4 are biased and operate as pull-ups. Q5 functions as a resistor, and Q6 works as a diode to bias Q3 and Q4. To construct a diode, the gate and source of transistors Q7 and Q8 are connected. This configuration results in a diode with an improved voltage-to-current characteristic curve. The Min operator is simulated in PSPICE using the TSMC 180 nm library, and results are reported in Fig. 10.

In Fig. 10 (a), the binary simulation operates like a binary logic AND gate. In Fig. 10(b), seven-valued logic is simulated; in Fig. 10(c), decenary logic is shown, and in Fig. 10(d), analog inputs

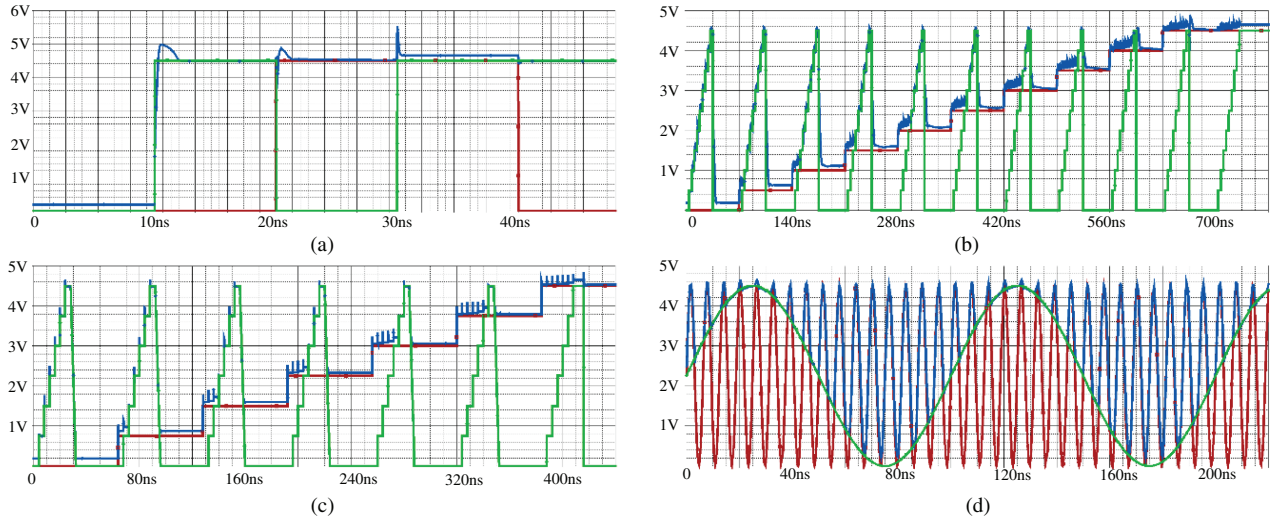

Fig. 7. Max operator 180 nm simulation (a) Binary (b) Ten valued (c) Seven valued (d) Analog (Red & Green inputs, Blue output)

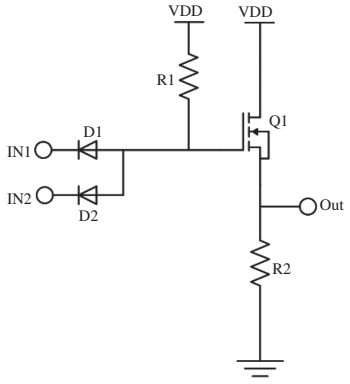

Fig. 8. Discrete Min operator's circuit

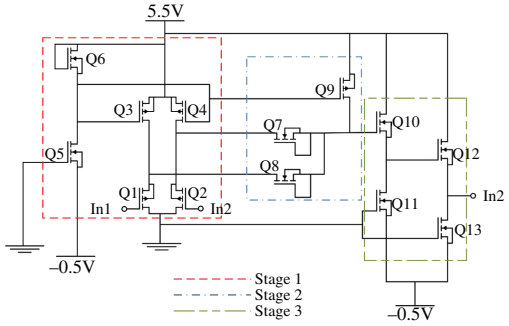

Fig. 9. Min operator in TSMC 180 nm

are simulated. Similar to the Min operator, the Max operator uses only 13 transistors (not exactly the same number of transistors) and operates in analog mode. The simulation results demonstrate that this circuit can work with various analog and digital input signals. Figure 10 can be used as proof for some of the algebraic field axioms, such as Closure, Commutativity, and Identity. In the reported experiment, nearly all possible input conditions for the operator are generated.

8. Optimism Step and Pessimism Step Operator

Max and Min operators alone are not sufficient to build a universal logic family. To cover all output values for any desired input value and create a universal logical family, two more operators are added. The OS operator increases the input signal from any level to the upper level, except for level 9, which remains untouched. The circuits of the OS and PS operators are straightforward to understand.

Figure 11(a) and (b) display the PS and OS operator circuits, respectively. The OS circuit is the complement of the PS circuit and is implemented using PMOS transistors. Transistors Q4, Q5, and Q6 function as diodes to reduce power consumption. The OS and PS operators are compatible with other multi-valued logics with a 0.5 V step level.

Figure 12 shows the simulated results of the OS and PS operators.

9. Comparison against Other Logics/Technologies

To substantiate the superiority of the designed circuits, it is imperative to conduct a comparative analysis with a range of emerging technologies.

Max and Min operators have been compared versus binary FinFET 14 nm [34–37], binary FET 45 nm [38], ternary CNTFET 32 nm [39], Quaternary CNTFET 32 nm [40] and binary FET 130 nm [41] technologies.

A comparison of various technologies is presented in Table I. The implementation includes a 4-bit binary Max operator and a 4-bit comparator, both utilizing 174 transistors, as well as a 4-bit 2×1 multiplexer (MUX) requiring 56 transistors. In contrast, a 4-bit Max operator in binary technology necessitates 230 transistors.

Figure 13(a) depicts a 4-bit binary comparator circuit, while Fig. 13(b) illustrates a one-bit binary 2×1 MUX. To facilitate a comparison between ternary [39] and quaternary [40] MVL against decenary Min and Max operators, it is necessary to design ternary and quaternary operators with identical operations and input/outputs. For this purpose, using an MVL comparator and three MVL 2×1 MUXs, ternary and quaternary-based Max operators are designed. The block diagram for a MVL Max

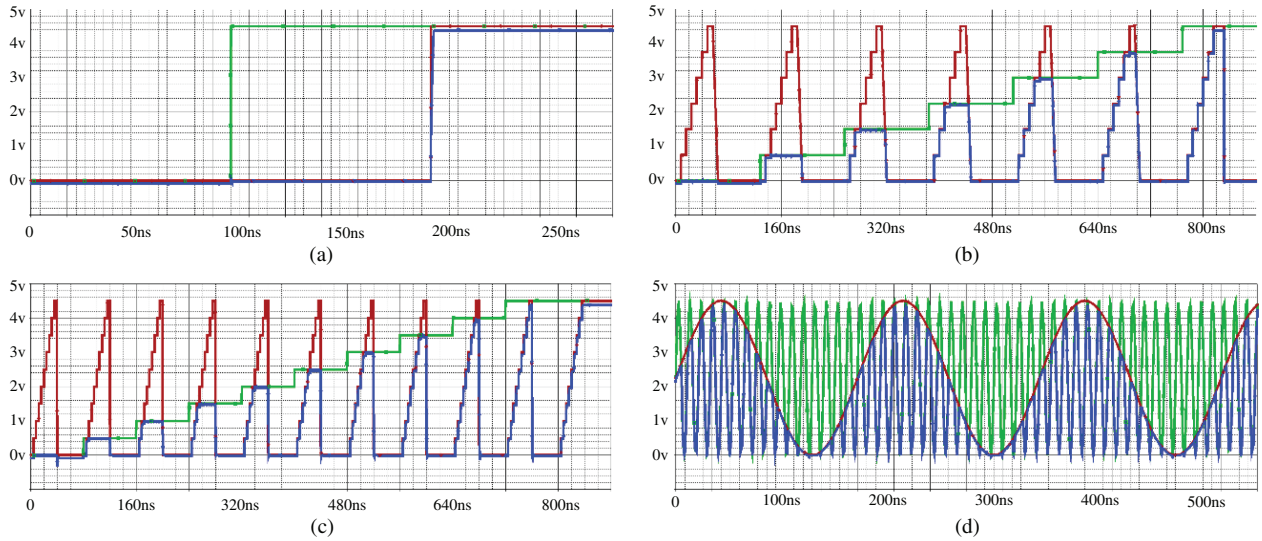

Fig. 10. Min operator 180 nm simulation (a) Binary (b) 7 valued (c) 10 valued (d) Analog (inputs are in Red & Green, output is in Blue)

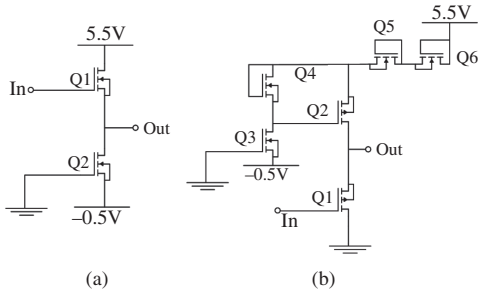

Fig. 11. (a) OS circuit (b) PS circuit

operator circuit based on ternary and quaternary logics are depicted in Fig. 14.

Table I compares the proposed technology against other documented technologies, considering three properties for Min and Max operators.

1. Complexity of the circuit, i.e., number of transistors within the operator's circuit.
2. Power dissipation for the operator.
3. Propagation delay for the operator.

In terms of complexity, the proposed decenary Max and Min operators exhibit approximately 16 times better performance than other circuits. On the other hand, Table I indicates that the proposed decenary circuits do not outperform their binary 14 and 45 nm or ternary 32 nm counterparts in terms of power dissipation. However, when compared to 130 nm technology, the proposed technology remains competitive in power dissipation. The propagation delay in the proposed technology is superior to that of the most compared technologies, with only the quaternary 32 nm technology demonstrating faster performance.

The reported work is based on 180 nm silicon devices, and the use of smaller scale FETs is currently not feasible due to limitations with the breakdown voltage.

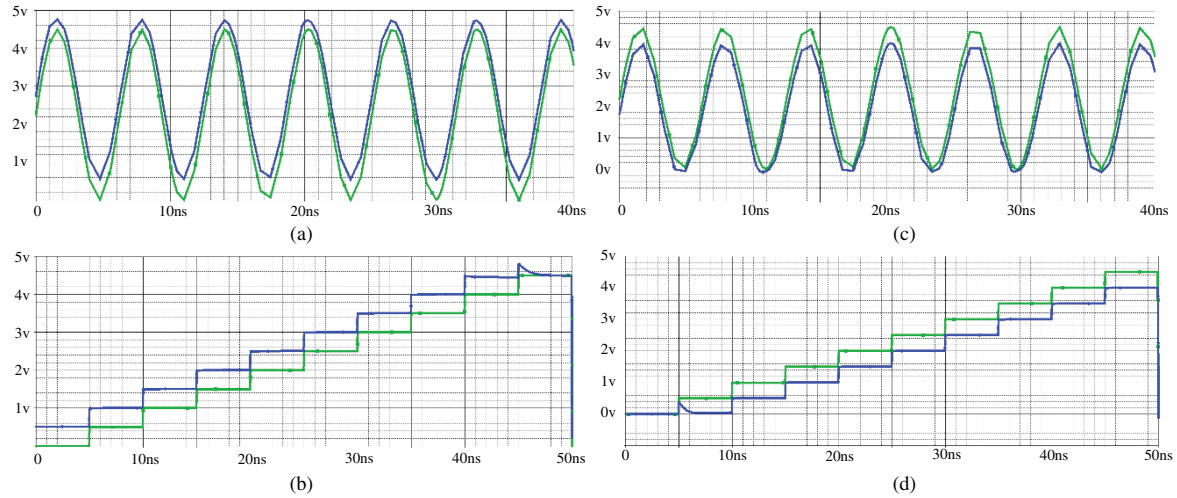

Fig. 12. OS simulation (a) Analog (b) 10-valued and PS (c) Analog (d) 10 valued (input is in Green, output is in Blue)

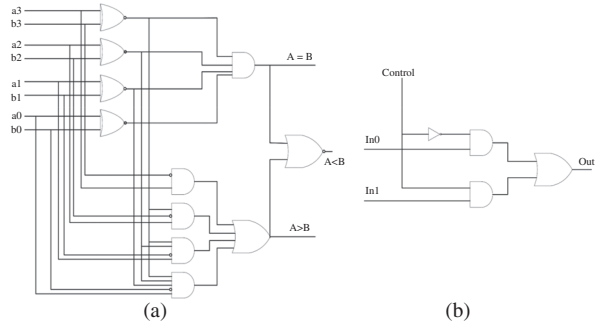

Fig. 13. Binary cricuit (a) 4 bit binary comparator (b) Binary MUX 2×1

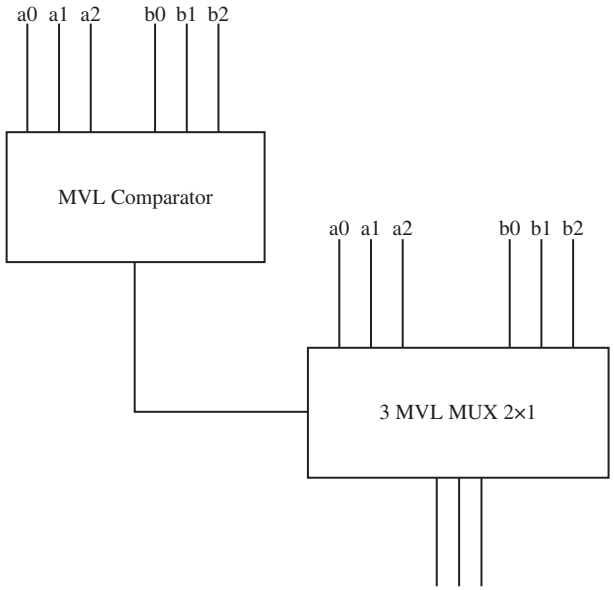

Fig. 14. MVL Max (ternary and quaternary)

However, in recent years, a new technology known as Gallium Nitride (GaN) has emerged in the manufacturing of VLSI chips. This technology boasts a very high breakdown voltage and can accommodate very small-scale FETs. The substrate for this technology is GaN. Despite its potential, this technology was not utilized in the reported work due to the inaccessibility of the GaN transistors library at that time. In the work reported by Ture *et al.* [42], a 100 nm MOSFET with a 60-V breakdown voltage was presented.

It should be noted that when comparing decenary against quaternary systems, the overall performance of the operations is directly dependent on the size of the numerical system used. The larger the size of the numerical operation, the higher its performance. The peak performance is achieved when the number of levels approaches infinity, as in the case of analog computing.

10. Conclusion

The present study introduces a novel universal family for decenary logic, supported by hardware implementation. The proposed circuitry operates in voltage mode and exhibits the following notable features.

Table I. Comparing the proposed decenary logic against a number of technologies

Used technology	Number of transistors	Power dissipation	Propagation delay
TSMC 180 nm Max operator	14	68 uW	3.43 ns
TSMC 180 nm Min operator	13	28 uW	3.1 ns
Binary FinFET 14 nm	230	2 uW	15-layer Gates = 3.55 ns
Binary 45 nm	230	3 uW	15-layer Gates = 6 ns
Ternary CNTFET 32 nm	384	3.12 uW	6 ns
Quaternary CNTFET 32 nm	240	60 uW	1.25 ns
Binary 130 nm	230	701.5 uW	24.6 ns

- Utilization of commercial MOSFET transistors for the implementation of the MVL family circuits.
- Transition from switching logic design to analog design.

The proposed approach is inherently analog, with circuit operation dependent solely on the number of input levels. The potential for an unlimited increase in logical input levels allows the system to function as an analog computer. A distinctive aspect of this work is the introduction of a comprehensive set of logical operators, constituting the D-MVL family. This family includes the Max operator, Min operator, PS, and OS circuits, which together complete the decenary logic set.

As detailed in Table I, the D-MVL family was designed using commercial TSMC 180 nm technology, operating in voltage mode and analog. The proposed technology demonstrates satisfactory performance, with favorable power consumption and speed that matches or exceeds other comparable MVL technologies.

11. Future Works

For future work, it is envisioned to explore computational circuits that integrate both logical and arithmetic functionalities. This will involve the development of circuits that not only support logical operations but also facilitate computational tasks, thereby expanding the capabilities of the proposed D-MVL family. The goal is to create a more versatile and robust system that can operate within a wider range of applications in digital and analog computing.

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