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Strategies for Next-generation CdTe Solar Cells: from Absorber Engineering to Tandem Integration

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Strategies for Next-generation CdTe Solar Cells: from Absorber Engineering to Tandem Integration

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PhD Thesis

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Abstract

Cadmium Telluride (CdTe) stands as the only thin-film photovoltaic technology that has achieved large-scale commercial success, offering a unique combination of high stability and low production costs. This thesis investigates several strategic pathways to further advance CdTe technology, focusing on absorber engineering, material sustainability, and next-generation tandem integration.

The incorporation of selenium into the CdTe has recently enhanced the performance of the solar cells to 23.1 %. The narrower band gap of the CdSeTe/CdTe absorber boosts the short-circuit current density; also, Se introduction increases the carrier's lifetime. Optimizing CdSexTe1-x band-grading is crucial for achieving high- performance CdTe photovoltaics. The initial study of absorber engineering revealed that CdSeTe/CdTe devices fabricated by evaporation, followed by vacuum annealing at 450 °C to mix CdSe and CdTe layers, is an important step to increase conversion efficiency.

Recognizing Tellurium as a rare earth element and to further reduce costs, the second part to the research is based ultra-thin CdTe absorbers (<1µm). The absorber material CdSeTe/CdTe has a high absorption coefficient of 10^4 cm^{-1}, can absorb approximately 90% of incident light having the thickness of ~1µm. By reducing the absorber thickness, the costs, the solar cells' environmental impact and material consumption are strongly limited. These ultra-thin designs not only minimize material consumption but also ensure compliance with RoHS regulations for indoor applications. we have fabricated different absorber thicknesses ranging from 0.5 mm to 0.8 mm to study ultra-thin absorbers for CdSeTe/CdTe solar cells. We analyze the impact of the thickness reduction on the electrical parameters of the devices. Currently, our best-performing ultra-thin CdSeTe/CdTe solar cell has an efficiency of 11 %.

Thus, studying the effects of Se introduction in ultra-thin CdTe absorbers is essential. To investigate Se concentration's impact on ultra-thin CdTe, we fabricated CdSeTe/CdTe devices with an absorber thickness of 0.8 µm by depositing different CdSe/CdTe ratios. Prior to this study, the group's best-performing ultra-thin CdSeTe/CdTe solar cells had achieved an efficiency of 11%. However, by optimizing the Se introduction and the 0.8 µm absorber thickness as described in this work, an improved efficiency of 12.8% has been reached. This study shows that Se intro duction in ultra-thin CdTe results in structural properties different from those of thicker absorbers, impacting the device performance.

The thesis further examines the critical $CdCl_2$ activation treatment, a fundamental process that transforms device efficiency from <1% to >10%. We study the effect of oxygen and inert nitrogen

during $CdCl_2$ activation process on Group V (Arsenic) doping. Finally, we emphasize the potential of CdTe in tandem applications. By developing high-performance bifacial CdTe cells with transparent back contacts, this work provides a scalable route to combine CdTe with commercially established silicon solar cells by making a tandem device for breaking the single-junction efficiency limit using two of the most stable and industrially proven photovoltaic materials available today.

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Dissemination of Work

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ABSTRACT SUBMITTED

M. Mukhtar, Elisa Artegiani, Alessandro Romeo. “Analysis of Bifacial CdTe Top Cells for CdTe/Si Tandem Applications”. Submitted in 43rd European Photovoltaic Solar Energy Conference and Exhibition

Elisa Artegiani, Sharmiladevi Ramamoorthy, Alessandro Veneri, **Mariyam Mukhtar** and Alessandro Romeo. “Comparison of Sb_2Se_3 thin films deposited by vacuum evaporation and vapor transport deposition” Submitted in 43rd European Photovoltaic Solar Energy Conference and Exhibition

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Chapter 1

Introduction

1.1 Solar Energy (a source of electricity)

The Sun is the ultimate source of solar energy, making it the foundation for many renewable energy systems, including solar electricity generation. As a star located at the center of our solar system, the Sun has been emitting energy for billions of years, and this energy can be harnessed in various forms to meet human energy needs.

The Sun emits 3.8×10^{26} watts of energy, more than the Earth's total energy consumption. Nuclear fusion reactions taking place in the Sun's core provide this energy. Massive amounts of energy are released as heat and light when hydrogen atoms fuse to generate helium. Radiation from the Sun travels through space as electromagnetic radiation, which includes infrared, ultraviolet, and visible light.

A significant amount of the Sun's energy is absorbed or dispersed by the atmosphere. However, if properly harnessed, even a little fraction that does reach Earth is sufficient to supply the world's energy requirement many times over.

The energy of the Sun is very plentiful. More energy from sunlight strikes Earth in 1 hour than all of the energy consumed by humans in an entire year [1]. This demonstrates how solar energy has the potential to be an almost infinite resource that is, if the necessary technology is in place to effectively capture and transform it.

Solar energy is a clean, green energy source, in contrast to fossil fuels, which emit carbon dioxide and other pollutants when they are burned to generate electricity. Solar energy generation is an essential part of attempts to mitigate climate change and minimize global warming because it doesn't produce any emissions, water pollution, or disturbance of habitat. Just a limited amount of pollution is only generated by the fabrication of solar energy collectors.

We can drastically reduce our reliance on fossil fuels, cut greenhouse gas emissions, and enhance air quality by switching to solar energy. Furthermore, the transition to solar power is critical to meeting sustainability targets and reducing the total environmental effect of human energy use.

From a quantum-mechanical perspective, sunlight is made up of photons, which carry energy. When these photons reach Earth, renewable energy sources like concentrated solar power (CSP) systems and photovoltaic (PV) cells may absorb them and turn them into electricity. The manufacturing of solar PV which directly converts sunlight into electrical power will be the main focus of this thesis.

1.2 Solar Radiation

With a star of a diameter of 1.39×10^8 km, about 98.6% of the solar system's mass is given by the sun. The sun is roughly 1.5 × 108 kilometers away from Earth on average, and it takes 8 minutes and 19 seconds for its light to travel that distance. The Sun's mass is mostly composed of the chemical element's hydrogen (about 74%) and helium (25%); trace of heavier atoms makes up the remaining mass [2, 3]. The earth's temperature and weather are derived from the energy that the sun provides also through photosynthesis, which sustains all life on the planet.

For all intents and purposes, the solar constant, which has a value of about 1.353 kWm^{-2}, is the amount of solar energy that reaches the earth's atmosphere's periphery [4]. The solar radiation received on a unit area which is exposed perpendicularly to the sun's rays at an average distance between the sun and the earth is used to estimate the solar constant.

1.3 The solar spectrum

The sun's electromagnetic radiation includes both ionizing (x-rays and gamma rays) and non-ionizing (UV, visible, and infrared). The spectrum of solar radiation is displayed in Figure 1.1.

The composition of the atmosphere and the length of the radiation's travel through it determine the radiation's intensity and spectral distribution as it reaches the earth's surface.

The main components of the present-day atmosphere are water, oxygen, and nitrogen (N_2). Approximately 78% of their composition is N_2, 21% is O_2, and 1% is made up of Ar (0.93%) and CO_2 (0.03%) [5].

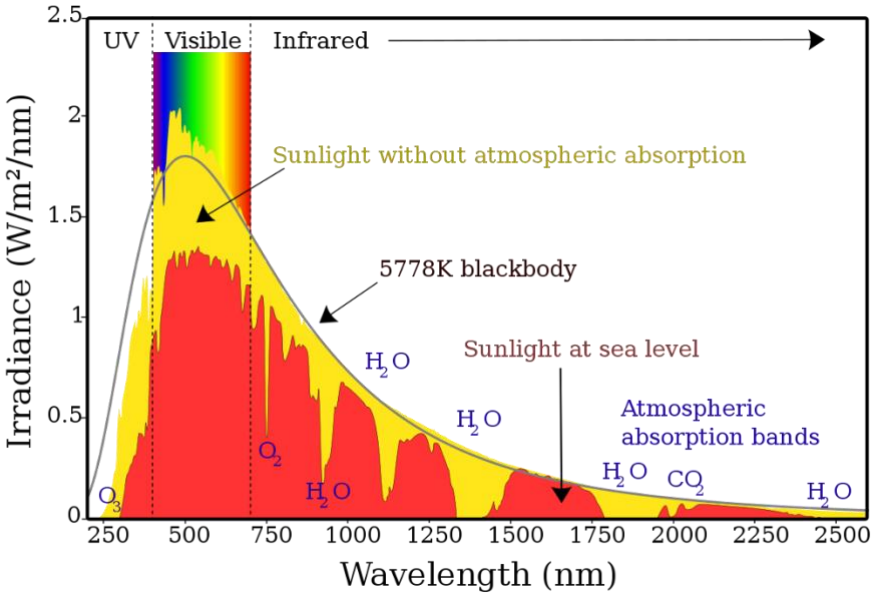

Figure 1.1: Spectrum of solar radiation [6]

The solar spectrum is divided into three major areas [3]:

1. About 5% of the irradiance is in the UV area.
2. About 43% of the irradiance is in the visible region.
3. About 52% of the irradiance is in the infrared area.

Some of the radiation from the sun is absorbed, some is reflected, and some is dispersed widely as it travels through the atmosphere. The longer sunlight travels through the earth's atmosphere, the more it is attenuated and the sun's spectrum is altered.

When the sun is directly overhead, the route length is at its shortest; as the sun descends farther in the sky, the path length grows. The word air-mass (AM) describes the length of the route through the atmosphere. It is described as the thickness of the air layer that surrounds the earth and through which sunlight passes. The length of sunlight's path through the atmosphere to the earth's surface is seen in Figure 1.2.

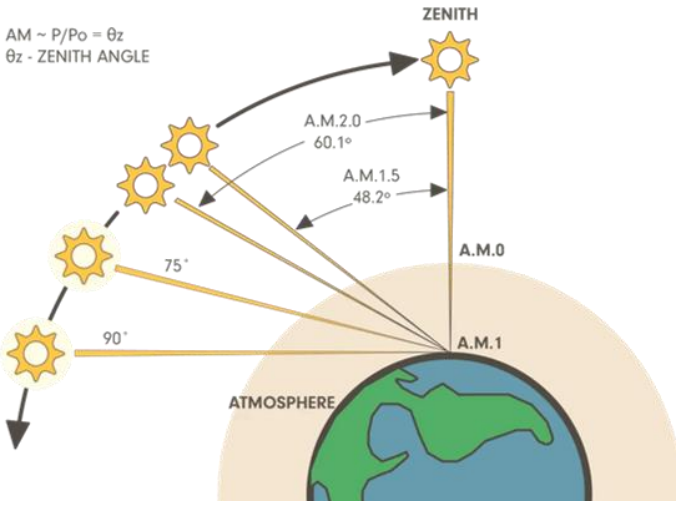

Figure 1.2: Path length of the sunlight through the atmosphere [7]

The air mass is defined as

$$AM = \frac{1}{Cos\theta_z} = sec\theta_z \qquad (1.1)$$

Where θ_z represent the angle between the sun and zenith.

When the sun is directly overhead, the spectrum received on Earth's surface is referred to as AM1.0. The power incident per unit area is assumed to be 925 Wm^{-2}. The most popular terrestrial

standard for assessing solar cells is the AM1.5 spectrum. It is the distribution of solar spectral irradiance incident at sea level from the sun at 48.2 degrees from the position normal. For AM1.5, the total incident power is around 100 Wm^{-2}.

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Chapter 2

The Rise of Photovoltaics: A Historical Overview

The photovoltaic effect was discovered in 1839 by French physicist Edmond Becquerel. He discovered that being exposed to light or radiation may create an electric current or voltage, a fundamental mechanism underlying solar energy. Around 1860, French mathematician Augustin Mouchot was among the first to investigate the practical application of solar power by developing sun-powered motors. In 1883, Charles Fritts developed the first solar cell by covering selenium with a thin film of gold (Figure2.1). This early cell had an energy conversion efficiency of only 1-2 percent.

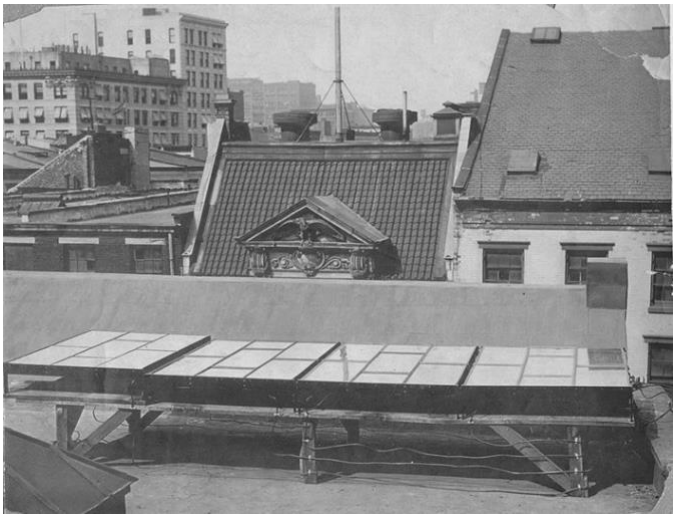


Figure 2.1: Charles Fritts installed the first solar panels on New York City rooftop in 1884.

The wet photo-electrochemical effect was used by early solar cells in the nineteenth century. To produce electricity from light, these cells generally employed silver chloride or copper oxides coatings on metal surfaces. In 1954, Bell Labs produced the first viable solid-state semiconductor solar cell, ushering in the era of high-performance solar energy conversion.

The infographic below depicts the history of solar cells from their initial stages to the modern technology employed today.

1800's

The discovery of Photovoltaic (PV) cells, the cells that power solar power, dates as far as the 1800s.

It all began when a nineteen-year-old French scientist, Edmond Becquerel was experimenting with an electrolytic cell composed of two metal electrodes.

1839 – Edmond Becquerel discovers PV effect.

1883 – An American inventor, Charles Fritts develops the first PV cell by putting selenium on a metal plate.

1877 – William Adams and Richard Day, both American scientists, publish "The action of light on selenium."

1888 – An American chemist, Edward Weston receives the first US Patent for Solar Cell.

1888 to 1891 – Aleksandr Stoletov develops the first solar cell using the outer photoelectric effect.

1900's

1901 – Nikola Tesla receives two patents for his radiant energy studies:
(1) Method of utilizing radiant energy.
(2) Apparatus for the utilization of radiant energy.

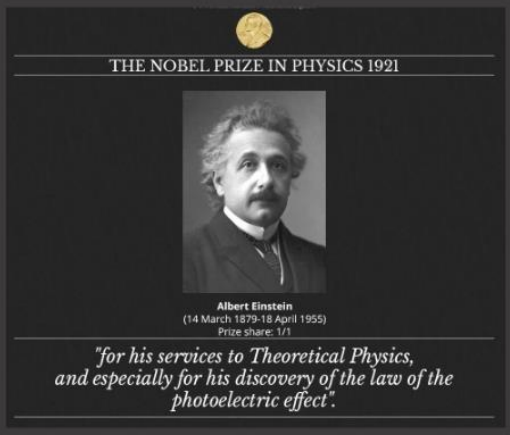
1904 – Wilhelm Hallwachs develops a semiconductor-junction solar cell.

1905 – Albert Einstein's theory of "photoelectric effect."

1916 – Robert Millikan supports Einstein's theory by providing proof.

1922 – Einstein receives Nobel Prize for his photoelectric effect theory.

1932 – Stora and Audobert discover a photovoltaic material, Cadmium Selenide.



1950's

1954 – An American research company, Bell Labs, showcases first high-power silicon PV cell that has about 6 percent of efficiency.

1955 – Western Electric begins commercialization of silicon PV system design technologies.

1958 – US Vanguard 1, the first solar-driven space satellite was launched. The U.S. Signal Corps Laboratories develops a radiation resistant solar cell. Hoffman Electronics' nine percent efficient solar cell.

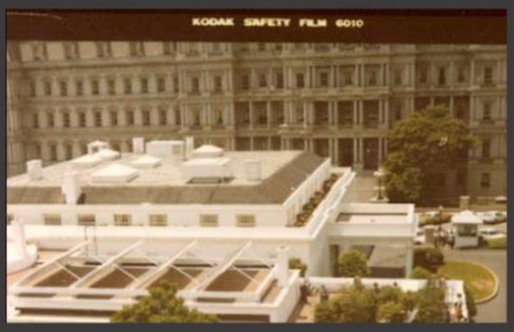
1960's

1960 – Hoffman Electronics forges a new solar cell with fourteen percent efficiency.

1963 – Sharp Corporation manufactures a feasible photovoltaic module of silicon solar cells; Japan enters the scene, installing a 242-watt PV array on a lighthouse.

1966 – NASA commences Orbiting Astronomical Observatory with a PV array.

1967 – Soyuz 1, the first solar-powered spacecraft,



1970's

1974 - J. Baldwin, at Integrated Living Systems, co-develops the world's first building (in New Mexico) heated and otherwise powered by solar and wind power exclusively.

1977 – The Department of Energy founded its Solar Energy Research Institute in Golden, Colorado. Solar panels were installed on the White House.

1980's

1980 – The first thin film solar cell was developed by the University of Delaware. It exceeded 10 percent efficiency.

1985 – The Centre for Photovoltaic Engineering develops a 20 percent efficient silicon cell.

1989 – Reflective solar concentrators are first applied with solar cells.

1990's

1991 – Development of the first Efficient Photo-electrochemical cell and the Dye-sensitized solar cell.

1992 – A 15.89 percent efficient thin-film CdTe solar cell created by the University of South Florida.

1994 – Japan starts “70,000 Solar Roofs” PV subsidy program.

1999 – 1000 megawatts of installed PV power.

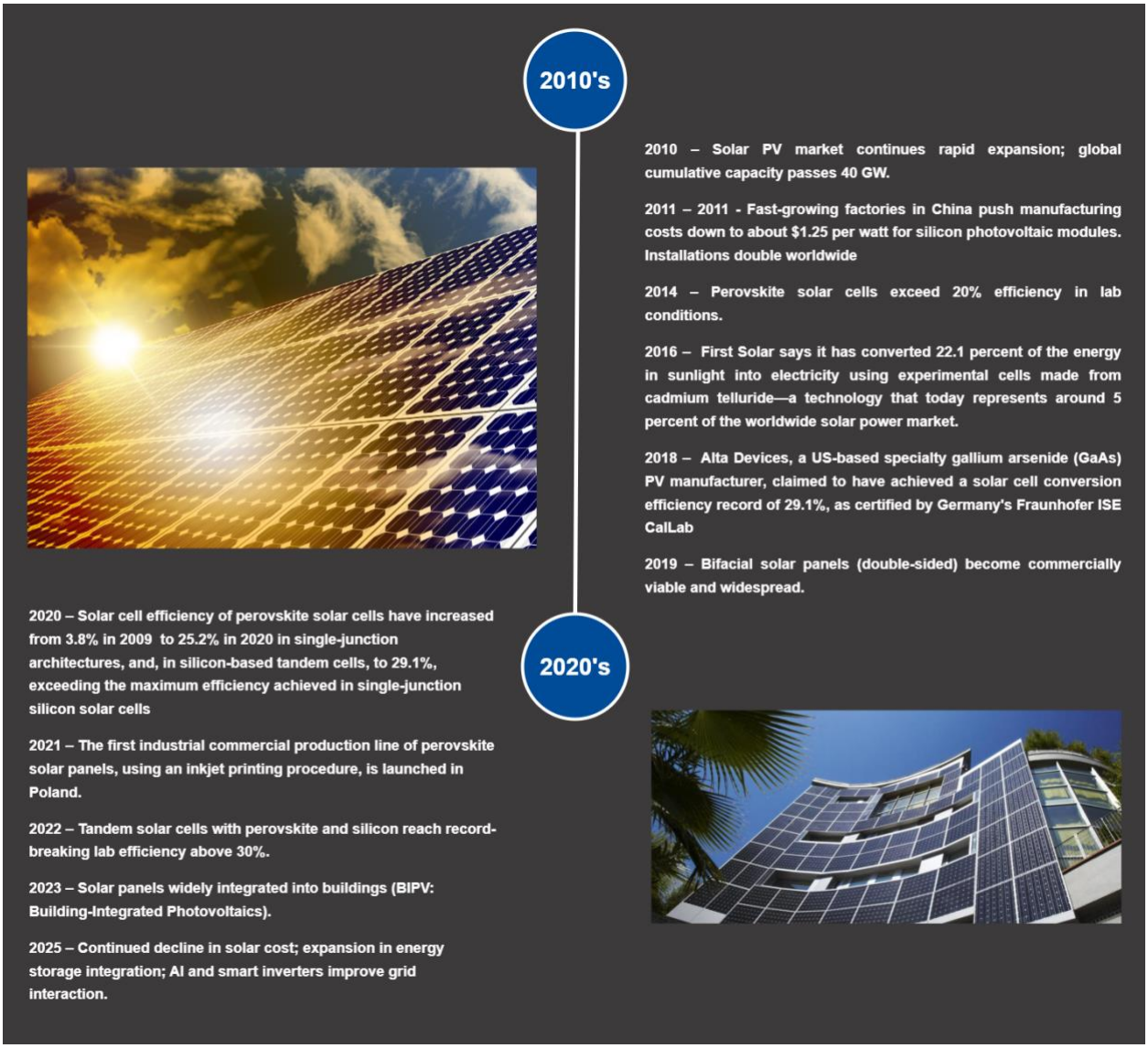
2000's

2006 – Solar cell advances, surpassing the 40 percent efficiency.

2007 – Google's Project Sunroof was launched.

2008 – The birth of the inverted metamorphic triple junction solar cell.

2010 – Modern solar panels installed on the White House.



The history of photovoltaics is marked by continuous innovation and progress, tracing the journey from early scientific discoveries to today's advanced solar cell technologies. The evolution can be broadly understood through four generations of solar cells, each reflecting the technological breakthroughs and changing priorities in the quest for efficient and affordable solar energy.

2.1 Generation of Solar Cells

The rapid advancement of photovoltaic (PV) technology over the last seven decades has been shaped by the dual objectives of improving energy conversion efficiency and reducing cost per watt. Solar cell development is commonly categorized into four successive generations, each defined by dominant material systems, structural innovations, and manufacturing methodologies. The first generation involves high-efficiency crystalline silicon devices, the second generation is focused on thin-film technologies for cost and flexibility, the third generation comes

from the exploration of emerging and unconventional structure to break efficiency barriers, and the fourth generation is currently integrating organic and inorganic hybrids and nanostructures for multifunctional, high-performance applications [1–3].

This generational framework not only helps in understanding the historical trajectory of PV development but also provides a roadmap for future research priorities. While the first generation remains the backbone of today's PV market, the subsequent generations reflect ongoing efforts to address the limitations of earlier designs such as material scarcity, fabrication complexity, and stability while capitalizing on opportunities provided by advances in materials science, nanotechnology, and manufacturing automation.

2.1.1 First Generation Photovoltaic Cells

First-generation PV cells rely on thick wafers of crystalline semiconductors, predominantly monocrystalline silicon, polycrystalline silicon, and gallium arsenide (GaAs). They are characterized by high efficiencies, long operational lifetimes exceeding 25 years, and proven large-scale manufacturability. Silicon-based solar cells alone account for over 80% of the global installed capacity, owing to their reliability and well-established supply chains [4–6]. Monocrystalline silicon cells are produced using the Czochralski method, yielding a continuous single crystal with minimal defects. This structural perfection enables carrier lifetimes sufficient to achieve efficiencies in the range of 15–24% under standard test conditions [7]. The band gap of 1.1 eV is near-optimal for terrestrial sunlight absorption, but efficiency declines at elevated temperatures due to increased recombination. Polycrystalline silicon cells are made via directed solidification, which results in ingots with numerous crystal grains. Although this method saves silicon waste and is more economical, recombination centers are introduced by grain boundaries, which results in lower efficiency, usually between 10% and 18%. However, advancements in anti-reflective coatings, passivation, and texturing have reduced the performance difference with monocrystalline devices. Thin film GaAs-based solar cells have demonstrated laboratory efficiencies of up to 29.1% [8]. Multi-junction systems utilizing GaAs have reached record efficiencies of more than 47% in focused sunlight. However, terrestrial deployment is limited because of the expensive cost of substrates and epitaxial growth.

Technological refinements in this generation include aluminum back surface field (Al-BSF) designs, which enhance rear-side reflectivity and reduce recombination losses, passivated emitter and rear cell (PERC) structure that further boost light trapping, and silicon heterojunction (SHJ) cells that integrate crystalline wafers with amorphous silicon layers to minimize interface recombination. With theoretical efficiency limits around 29.4%, first-generation technologies are now in a stage of incremental optimization.

2.1.2 Second Generation Photovoltaic Cells

Second-generation PV cells emerged in the 1980s as a direct response to the high material consumption and production cost of wafer-based devices. These thin-film cells use light-absorbing layers only 1–10 µm thick, deposited on inexpensive and/or flexible substrates such as glass, metal foils, or polymers. This structure reduces semiconductor usage by orders of magnitude compared to crystalline wafers. Amorphous silicon (a-Si) cells are among the earliest thin-film technologies, with efficiencies between 5% and 12%. Their high absorption coefficient allows for extremely thin active layers, and deposition can be carried out at low temperatures on flexible substrates. However, the Staebler Wronski effect [9], which induces light-induced degradation, remains a limitation.

Cadmium telluride (CdTe) cells have become the most commercially successful thin-film technology, with record efficiencies reaching 23.1% [10]. CdTe has a nearly ideal band gap of 1.45 eV for single-junction devices, allowing absorber layers as thin as 1 µm.

Copper indium gallium diselenide (CIGS) cells combine high absorption with tunable band gaps (1.0–1.7 eV) depending on the composition (In/Ga ratio). Efficiencies of 23.6% [11] have been achieved in the laboratory, and modules above 20% are commercially available.

Flexible CIGS modules have made possible uses in aircrafts [12], portable electronics, and building-integrated photovoltaics (BIPV). Kesterite ($Cu_2ZnSnS_xSe_{4-x}$) cells are non-toxic and earth-abundant, alternative to CIGS, with recent record efficiencies of roughly 14.9% [13]. While Kesterite seems promisinge in terms of sustainability, there are issues in regulating defect states and increasing open-circuit voltage.

Thin film fabrication methods include vacuum-based technologies such as thermal-evaporation and sputtering, as well as non-vacuum processes such as electrodeposition and solution coating. These processes open possibilities for high-throughput roll-to-roll manufacturing and integration into unconventional surfaces.

2.1.3 Third Generation Photovoltaic Cells

Third-generation PV technologies encompass a diverse range of emerging materials and structure designed to overcome the limitations of single junction devices. While strategies like multi-junction structure specifically aim to transcend the Shockley-Queisser limit for single-junction devices (above 30%) [14], other technologies in this category focus on low-cost fabrication, flexibility, and tunable optical properties.

These emerging technologies include organic solar cells (OSC), dye-sensitized solar cells (DSSC), perovskite solar cells (PSC), and quantum dot (QD) devices. Among these, perovskites and multi-junction cells push for higher efficiencies, while OSCs and DSSCs offer advantages in terms of cost-effectiveness and integration potential.

OSC devices, made of conjugated polymers or tiny molecules, are prized for their lightweight, semi-transparent and flexible. Early OSCs had modest efficiency (~3-5%), but current designs with non-fullerene acceptors have reached 14% for single-junctions and 17% for tandem arrangements. The major problem is to maintain stability in the presence of sunshine and oxygen.

DSSCs capture light using a mesoporous semiconductor covered with a molecular dye, with charge transfer aided by a liquid or solid electrolyte. They operate remarkably well under diffuse lighting, making them ideal for indoor applications. However, electrolyte leakage and photochemical instability have restricted large-scale use.

In less than a decade of study, PSC multijunction technology has made significant progress, with efficiencies of more than 34.6% [15]. Their ABX_3 crystal structure enables variable band gaps and high light absorption. The primary obstacles to commercialization are the presence of hazardous lead in high-performing formulations and environmental instability.

QD solar cells exploit size-dependent quantum confinement to tune absorption properties. They have reached 17% efficiency, but many rely on lead-based materials, raising environmental concerns. Multi-junction (or tandem) devices achieve superior performance by vertically stacking multiple sub-cells with decreasing bandgaps. The top sub-cell has a wide bandgap to absorb high-energy photons while allowing lower-energy photons to pass through to the narrower bandgap sub-cells below.

This structure minimizes thermalization losses, as photons are absorbed by materials better matched to their energy. These sub-cells are typically connected in series via tunnel junctions heavily doped layers that allow electrons to quantum mechanically tunnel between the valence band of one cell and the conduction band of the next with low resistance. This requires precise current matching between layers to ensure optimal device performance. Such devices currently hold the world record for efficiency at over 36% under standard illumination.

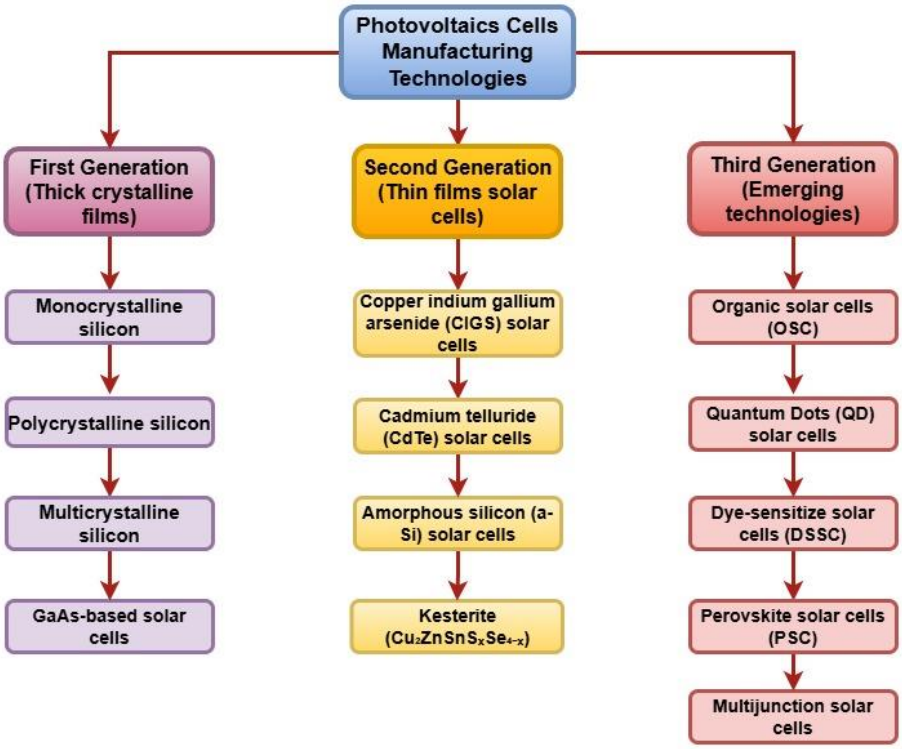


Figure 2.2: Solar cells generation and different solar types of solar cells

Solar cells generations framework illustrates not only the historical evolution of PV technology but also the diverse strategies pursued to meet global energy needs. First-generation crystalline silicon devices dominate the current market, while third-generation devices hold the promise to reach theoretical limits through novel materials [1–3]. However, these emerging technologies often face significant challenges regarding long-term stability and scalable manufacturing.

In contrast, second-generation CdTe technology has established itself as the most commercially successful thin-film candidate, offering a unique balance of high efficiency, low production costs, and proven field reliability. Despite its commercial success, CdTe devices have not yet reached their theoretical efficiency limit, leaving substantial room for improvement through material optimization.

Therefore, the next chapter will focus on the material properties, fabrication techniques, and characterization methods employed in CdTe-based devices, setting the stage for the experimental investigations of this research.

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Chapter 3

Background

Having established the historical context of solar cell generations, it is essential to understand the fundamental physical principles that govern their operation. This chapter details the physics of the p-n junction, carrier generation, and recombination mechanisms. Understanding these fundamental interactions is a prerequisite for analyzing the specific loss mechanisms such as carrier recombination and depletion width limitations that will be investigated in the experimental chapters of this thesis.

3.1 Fundamentals of Electronic Materials

Electrons in individual atoms occupy distinct energy levels defined by quantum mechanics. When a large number of atoms combine to create a solid, their outermost electron wave functions overlap, which causes these separate levels to divide into several closely spaced layers. The Pauli exclusion principle, which forbids two electrons from occupying the same quantum state, causes these levels to combine into continuous energy bands.

The valence band comprises electrons that are tightly bound to atoms and responsible for chemical bonding, whereas the conduction band has energy levels where electrons can easily flow and contribute to electrical conduction. The distance between these bands, known as the band gap, describes a material's electrical characteristics. When the valence and conduction bands overlap, as they do in metals, electrons can travel freely, resulting in high conductance.

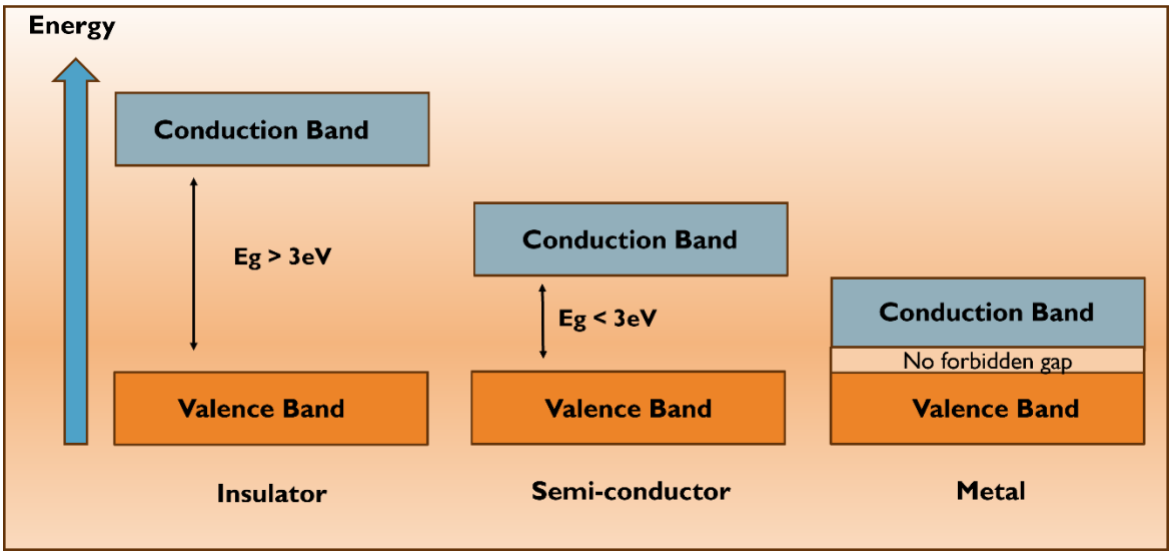

Figure 3.1: Band diagram of insulator, semiconductor and metal.

Insulators have large band gaps, generally larger than 3 eV (figure 3.1), therefore electrons need much more energy to leap to the conduction band, rendering electrical conduction inefficient.

Semiconductors like silicon and cadmium telluride (CdTe) lie between these extremes, with moderate band gaps (about 1.12 to 1.45 eV), which allows electrons to be thermally or optically excited, giving semiconductors-controlled conductivity. At absolute zero, all electrons occupy the lowest energy states, and the Fermi level, an energy level where the probability of finding an electron is 50%, helps distinguish conductors, insulators, and semiconductors by their position relative to the bands[1].

3.2 Semiconductors

Semiconductors are categorized as intrinsic or extrinsic based on the material band gap and impurity levels. An intrinsic semiconductor is a pure crystal without any added impurities. Thermal energy can excite electrons from the valence band to the conduction band, producing equal numbers of free electrons and holes. In such materials, the Fermi level typically sits near the center of the band gap as shown in figure 3.2.

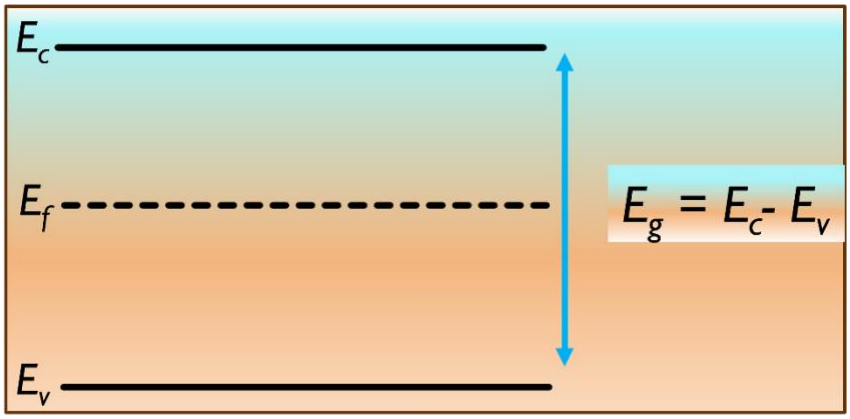

Figure 3.2: Energy bands for an intrinsic material. The Fermi level is in the middle of the gap.

However, semiconductors are intentionally doped by adding small quantities of impurities to improve conductivity and control whether electrons or holes dominate. A hole is defined as an electron vacancy within the valence band of the crystal lattice. Although it is physically the absence of an electron, this vacancy behaves effectively as a positively charged quasiparticle. When an electron from a neighboring atom moves to fill the vacancy, the vacancy itself shifts position. This relative movement allows holes to transport charge through the lattice, contributing to electrical current.

When donor atoms, which have one more valence electron than the host, are introduced, they add extra electrons that are weakly bound and easily excited into the conduction band. This results in an n-type semiconductor, where electrons become the majority carriers. Consequently, the fermi level defined as the energy level where the probability of finding an electron is 50% shifts closer to the conduction band. Conversely, acceptor atoms, which have one fewer valence electron, create holes by accepting electrons from the valence band. This leads to a p-type semiconductor with holes as majority carriers, shifting the Fermi level toward the valence band shown in figure (3.3).

This precise control over carrier concentration and conduction type through doping forms the basis for creating semiconductor junctions. Such junctions are the heart of most electronic and optoelectronic devices, including solar cells, enabling the separation and collection of charge carriers generated by light absorption[1].

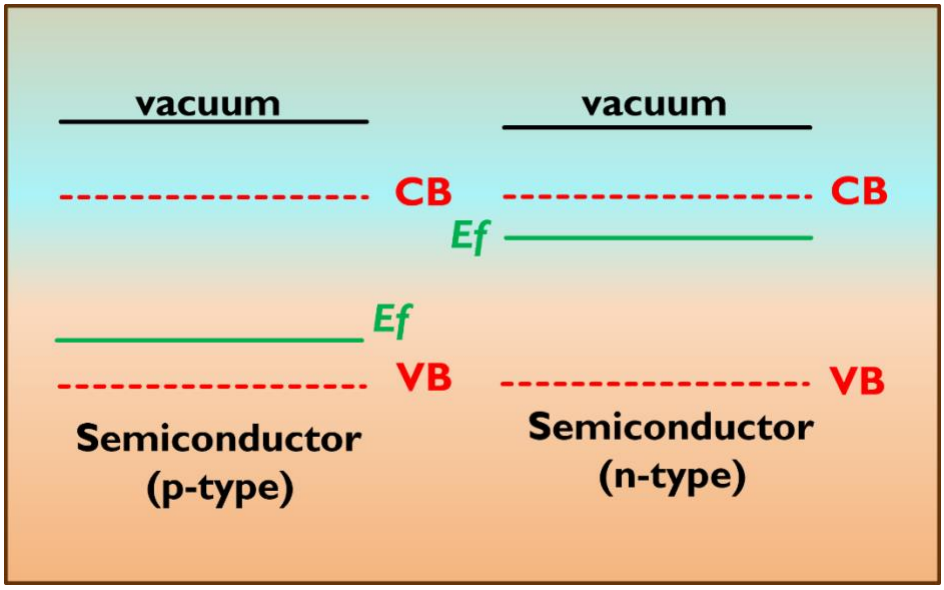

Figure 3.3: Shift in the Fermi level for different types of dopants. The n-type impurities push the Fermi level up towards CB, whereas p-type impurities lower it down towards VB.

3.3 Semiconductor Junctions

According to semiconductor physics, the operation of all electronic and optoelectronic devices depends on the formation of junctions between regions with different electrical characteristics. The properties of these junctions determine how charge carriers (holes and electrons) are generated, separated, transported, and collected within a device. Junctions can assume a variety

of configurations based on the materials and doping levels used, each offering distinct benefits. Broadly, semiconductor junctions are classified into homojunctions and heterojunctions. Additionally, the interface between a metal and a semiconductor forms specific contacts known as Schottky or Ohmic contacts.

3.3.1 Formation of P-N Junction

The most basic and widely used junction is the p–n junction, which arises when a p-type semiconductor (containing majority of holes) and an n-type semiconductor (containing majority of electrons) are brought into contact as shown in figure 3.4 (a). As soon as these two regions are joined, carriers begin to diffuse: electrons from the n-side move into the p-side, and holes from the p-side move toward the n-side (fig 3.4 (b)).

This diffusion leads to recombination near the interface and results in a region depleted of mobile charge carriers. Only fixed ionized donor and acceptor atoms remain in this region create an internal electric field (figure 3.4 (c)). This field gives rise to the built-in potential, which counteracts further carrier diffusion and brings the system into thermal equilibrium creating what is known as the depletion region (figure 3.4 (d)).

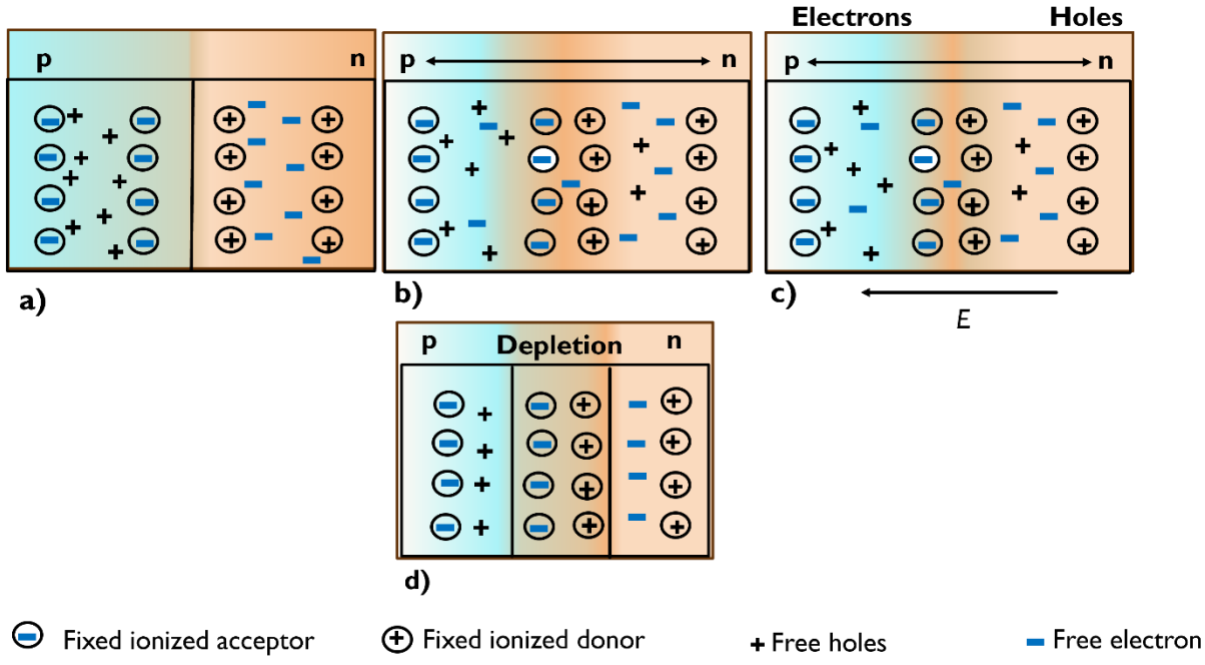

Figure 3.4: Formation of a p-n junction. a) P-type semiconductor grown next to the n-type semiconductor. b) Diffusion of free carriers. c) Electric field is created and balances the diffusion current. d) Equilibrium.

At equilibrium, the Fermi level becomes flat across the junction, and the energy bands bend in response to the built-in electric field. While the p–n junction plays a central role in many devices, it is just one example of how semiconductors can be joined.

In forward bias, the external voltage reduces the built-in potential, allowing carriers to cross the junction easily and produce a large current.

In reverse bias, the potential barrier increases, carrier flow is suppressed, and only a small leakage current persists. This asymmetric response to voltage is the foundation of diode behavior. It also makes the p–n junction so effective in separating photogenerated carriers in photovoltaic devices.

The p-n junction plays an important role in the operation of solar cells. When lighted, photons absorbed in or around the depletion area drive electrons to the conduction band, causing holes in the valence band. The internal electric field pushes electrons toward the n-side and holes toward the p-side, resulting in a photocurrent. The efficacy of this process is determined by the width of the depletion zone, the strength of the electric field, and the quality of the junction contact. Any deficiencies, such as traps, defects, or poor band alignment, can lead to radiative, recombination, auger recombination and Shockley-Read-Hall recombination (fig 3.5), which lowers the device's overall efficiency[2].

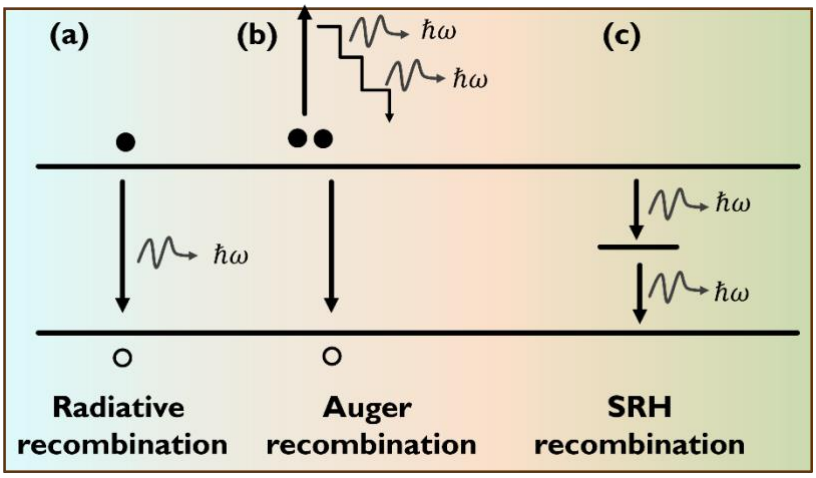

Figure 3.5: (a) Radiative recombination (b) Auger recombination (c) SHR recombination

3.3.2 Homojunction and Heterojunction

A p-n junction can be a homojunction or heterojunction. A homojunction occurs when a material is doped with two distinct dopants shown in figure 3.6 (for example, a p-n junction in silicon). These junctions benefit from flawless lattice continuity, which reduces interface recombination and allows for consistent electrical activity. However, the limits of a single material system,

particularly optical absorption and band gap adjustment, have resulted in the creation of more complicated systems [2].

To overcome such limitations, heterojunctions have been considered. Heterojunctions, which combine two semiconductor materials with differing band gaps and electron affinities, allow for fine control over band alignment, recombination and carrier injection shown in figure 3.7. However, this interface creates new problems, such as defect states and lattice mismatch, which may hold charge carriers and limit device performance. In thin-film CdTe solar cells, for example, the junction is commonly constructed between p-type CdTe and n-type CdSe, resulting in a heterojunction optimized for optical absorption and effective charge separation.

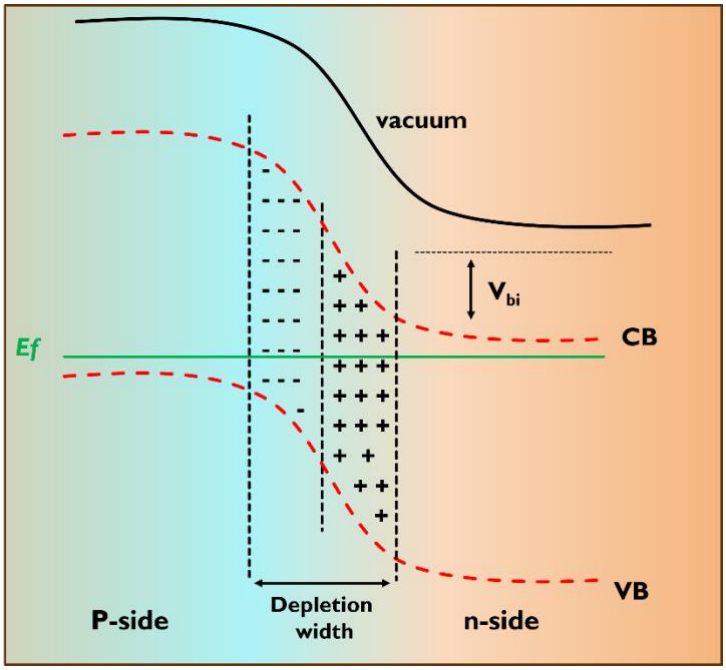

Figure 3.6: Energy band diagram of the p-n homojunction. Fermi levels must align at the same level.

One is the metal-semiconductor interface. Depending on the relative work functions of the metal and the semiconductor, the junction can behave as a Schottky barrier or form an ohmic contact. Schottky barriers are rectifying in nature and are used in fast-switching applications. At the same time, ohmic contacts are designed to provide minimal resistance to carrier flow, which is essential for efficient current collection in solar cells and electronic devices.

Further complexity is introduced with structures such as the p–i–n junction, in which an intrinsic (undoped) semiconductor layer is sandwiched between p-type and n-type regions. This intrinsic

layer widens the depletion region and enhances the electric field, improving carrier separation and collection, especially in devices where the absorber layer is thin or has a high defect density. Such structures are commonly used in amorphous silicon and some perovskite-based solar cells[2].

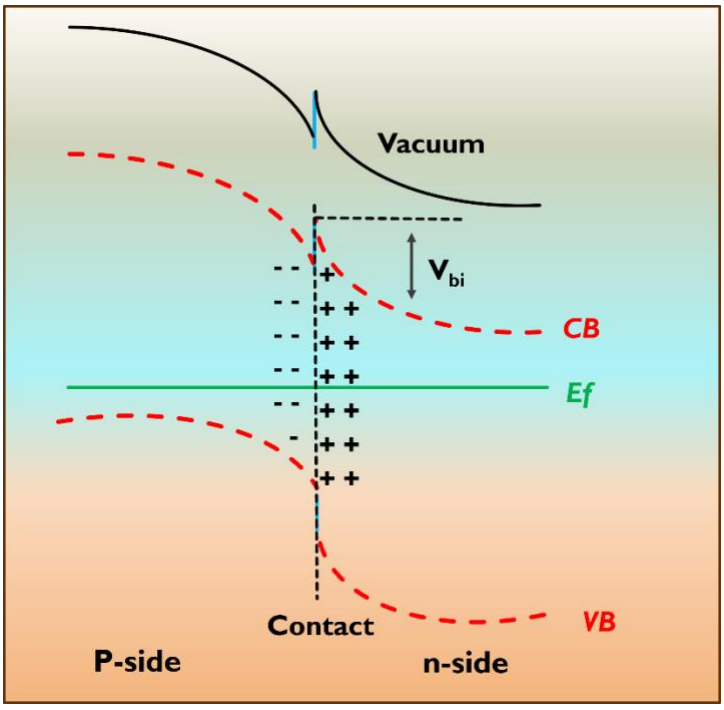

Figure 3.7: Example of the energy band diagram for a p-n heterojunction.

3.3.3 Metal-Semiconductor Junction

This junction is created at the interface between a metal and a semiconductor. The vacuum level is used as the reference energy for all other levels. A p-type semiconductor and a metal prior to contact, the work function of the metal (Φ_m) is assumed to be lower than that of the semiconductor (Φs), satisfying the condition:

$$\Phi_m < \Phi_s \qquad (3.1)$$

To align the Fermi levels, holes diffuse from the semiconductor into the metal, leaving behind negatively charged acceptor atoms. These immobile charged atoms create a depletion region on the semiconductor side. The resulting internal electric field creates a potential barrier known as Schottky barrier (shown in figure 3.8) that prevents further hole flow across the junction.

For a p-type semiconductor, the barrier height (ΦBp) is given by:

$$\Phi Bp = Eg - (\Phi m - Xs) \qquad 3.2$$

where Eg is the bandgap and Xs is the electron affinity of the semiconductor.

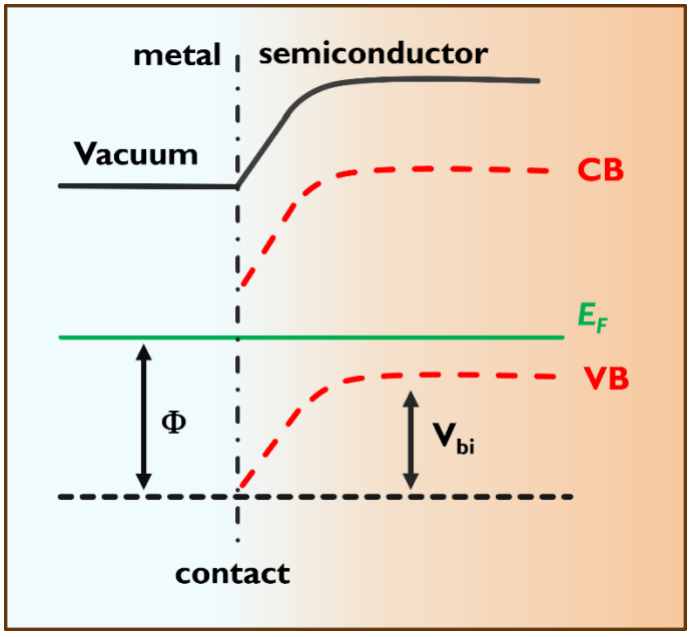

Figure 3.8: The energy band alignment after contacting metal and p-type semiconductor showing the Schottky barrier.

For a p-type semiconductor, an ideal ohmic contact occurs when the work function of the metal (Φ_m) is greater than that of the semiconductor (Φs).

$$\Phi_m > \Phi_s$$

The energy band alignment for this state is shown in Figure 3.9. Because the metal Fermi level is lower than the semiconductor Fermi level, holes are free to move from the valence band into the metal without encountering a potential barrier. This results in unimpeded hole flow and linear current-voltage (I-V) characteristics.

However, a good ohmic contact can still be achieved by allowing carriers to tunnel through the Schottky barrier. This is accomplished by heavily doping the semiconductor interface (p+). As shown in Figure 3.10, increasing the doping concentration significantly reduces the width of the depletion region (the barrier width). If the barrier becomes thin enough, charge carriers can tunnel through its quantum mechanically, even if a potential barrier height exists.

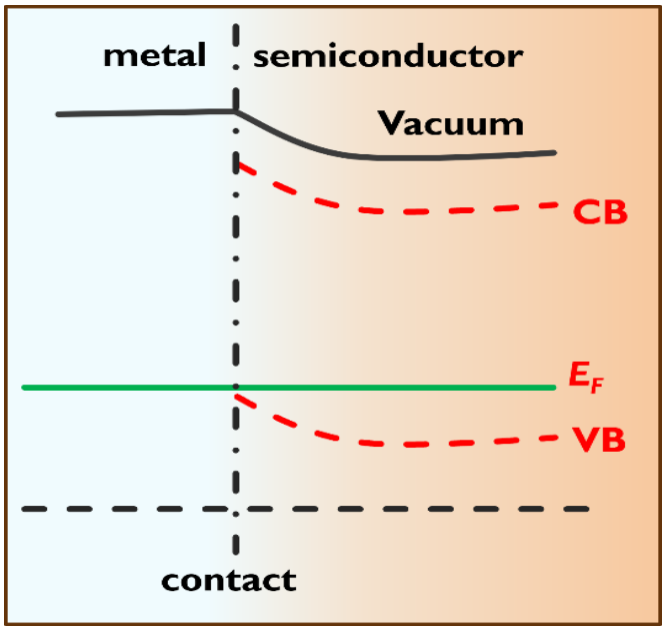

Figure 3.9: The energy band alignment after contacting metal and p-type semiconductor showing the Ohmic barrier.

As CdTe has a high work function, forming a good ohmic contact is challenging. Therefore, before metallization, the back surface is typically heavily doped (e.g., using Copper or creating a Te-rich surface) to narrow the barrier and facilitate hole tunneling.

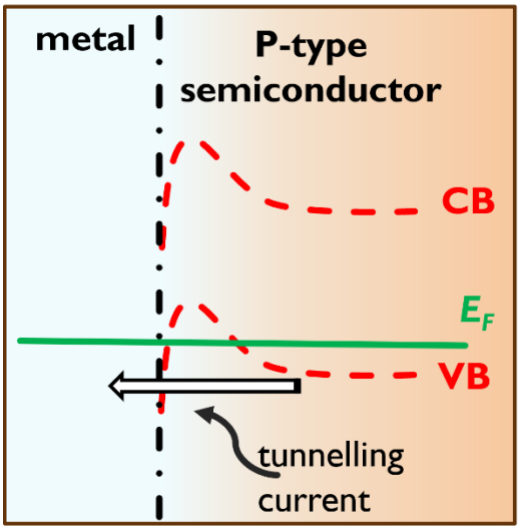

Figure 3.10: Changing Schottky contact to an Ohmic one by creating high density of localized states within the energy barrier.

Similarly, the reverse is the case for n-type semiconductor. In this case $\boldsymbol{\Phi_m > \Phi_s}$**.** The built-in potential (V_{bi}) and the electron barrier height Φ_{bi} are given by

$$\boldsymbol{V_{bi} = \Phi_m - \Phi_s} \qquad (\mathbf{3.3})$$

And

$$\boldsymbol{\Phi_{bi} = \Phi_m - \mathrm{X}} \qquad (\mathbf{3.4})$$

where χ is the electron affinity of the semiconductor.

3.4 References

[1] Unit 1 Band Theory of Solids 1.1Introduction. (1909). *Advanced Engineering Materials*, 1–30.

Chapter 4

The Photovoltaic Effect and Solar Cell Operation

The photovoltaic effect describes voltage and current generation in a semiconductor when it exposed to light. Photons with energy equal to or greater than the band gap are absorbed, exciting electrons into the conduction band and creating corresponding holes in the valence band.

Under the influence of the built-in electric field at the p–n junction, these carriers are swept in opposite directions, electrons toward the n-type layer and holes toward the p-type layer, creating a current if the circuit is closed. This process is reflected in a current voltage (J–V) characteristic.

Solar cells use the photovoltaic effect to turn light into energy. This process is divided into three stages: the sun's light is absorbed, carriers are created, and an external electric circuit selectively collects them.

4.1 Photogeneration of Carrier

Most solar cells are made from semiconductor materials to convert sunlight into energy. These materials have an energy structure where electrons are confined to specific energy levels. The lower energy level is the valence band (Ev), where electrons are tightly bound, and the conduction band (Ec) is the energy level where electrons can move freely. The space between these two bands is called the bandgap (Eg).

When light hits the surface of the solar cell, some of it may reflect off the surface depending on the material's properties; some may pass through, or some may be absorbed.

If the energy of the incoming light (photon) is less than the bandgap, it will pass through. However, it will be absorbed if the photon energy is equal to or greater than the bandgap. The amount of light absorbed depends on the material's ability to absorb it (absorption coefficient) which is also connected to the band structure.

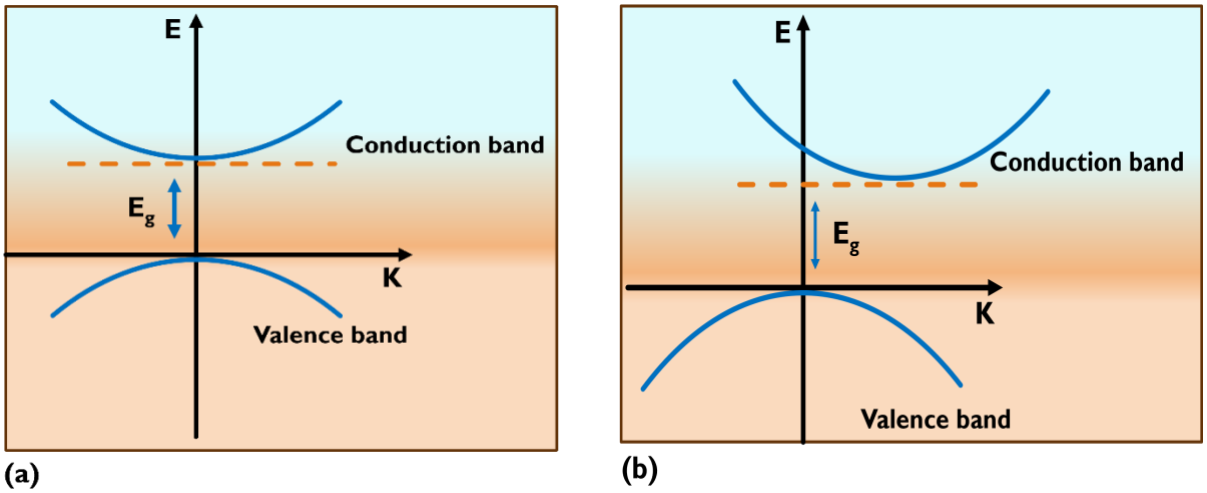

Figure 4.1: A schematic of (a) direct and (b) indirect transition in semiconductors.

If the valence band maximum (VBM) and conduction band minimum (CBM) of a material's band structure are at the same position in momentum space, electrons can transit between them by absorbing or releasing a photon. This material is referred to as a direct band gap semiconductor (figure 4.1(a)).

In contrast, an indirect band gap material contains VBM and CBM at distinct momentum positions (figure 4.1 (b)). As a result, electron transitions in these materials necessitate the use of a phonon (a quantum that represents a vibration of the crystal lattice) to assist conserve momentum. Direct band gap materials are particularly beneficial for solar cells because they absorb light more effectively, making them perfect for converting sunlight into power.

The absorption coefficient (α) also indicates the depth of light penetration before absorption, influencing the thickness of solar cells. When a photon is absorbed, its energy is transmitted to the material, and an electron moves from the valence band to the conduction band, forming an electron-hole pair (Fig. 4.2 (a and b)).

4.1.1 Separation of Charges

Once an electron–hole pair is generated within the depletion region of a p–n junction, the built-in electric field inherent to the junction rapidly separates the pair: electrons are driven toward the n-side and holes toward the p-side by drift motion. These carriers are then collected by the respective metal contacts. Conversely, if the photogenerated carriers originate in the quasi-neutral regions of the p-type or n-type semiconductor, they primarily undergo diffusion.

Through this process, carriers move toward the depletion region. Upon reaching in the depletion region, they are separated by the internal electric field and subsequently transported to the external circuit by drift, contributing to the photocurrent.

4.1.2 Collection of Carriers

The carriers are collected by moving toward the electrical contacts (fig 4.2 (c)). These contacts are located on opposite sides of the device. The efficiency of the collected carriers depends on the diffusion length, which needs to be long enough to reach the depletion region and help produce current. However, recombination losses will reduce the possibility of carrier's collection.

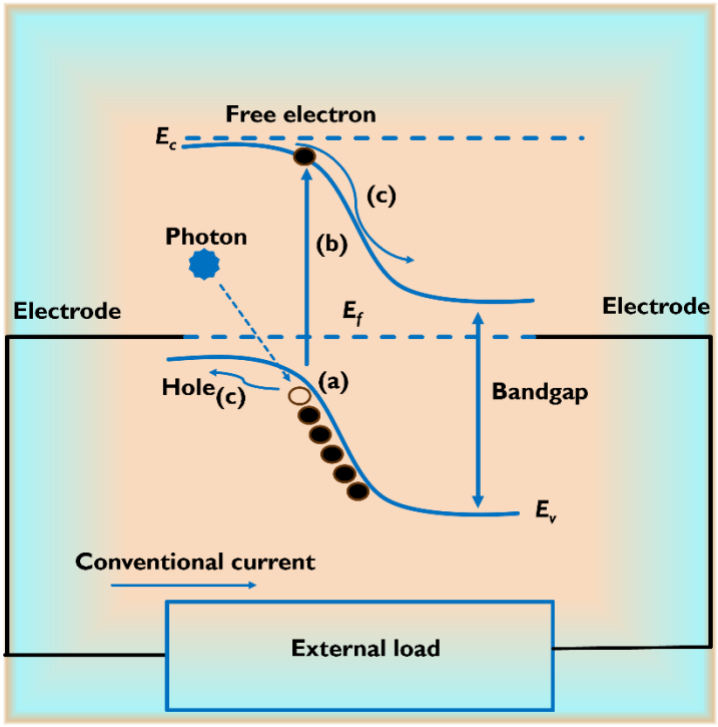

Figure 4.2: Photovoltaic effect. Light is absorbed by the semiconductor and makes electrons to gain enough energy to jump from the valence band to the conduction band. Charges are circulated through and external circuit by the use of contacts.

4.2 Solar Cell Performance

From the illuminated current–voltage (J–V) characteristics of a solar cell, we can extract several critical parameters that define the device's performance.

At its core, the solar cell behaves like a diode in the dark, and its current is modeled using the Shockley diode equation:

$$I = I_o(\exp\left(\frac{qV}{nkT}\right) - 1) \qquad (4.1)$$

where I_o is the reverse saturation current, q is the elementary charge, V is the voltage across the cell, n is the ideality factor, k is Boltzmann's constant, and T is the absolute temperature.

When the cell is exposed to light, a photocurrent (I_L) is generated, which modifies the current–voltage relationship to:

$$I = I_o\left(\exp\left(\frac{qV}{nkT}\right) - 1\right) - I_L \qquad (4.2)$$

This expression captures the total output current under illumination and forms the basis of the solar cell's J–V curve.

One of the most fundamental parameters is the short-circuit current density (Jsc), which corresponds to the maximum current per unit area the device can deliver when the terminals are shorted (i.e., when the voltage across the cell is zero). Jsc measures how well the device transforms incoming photons into charge carriers and how effectively those carriers are collected. It is controlled by the active layer's light absorption efficiency, carrier lifetime, and the amount of recombination losses in the bulk and at interfaces.

While Jsc indicates the current output, the open-circuit voltage (Voc) indicates the voltage potential that a device can create under illumination when no external current is applied. Voc is determined by the difference in quasi-Fermi levels of electrons and holes and is directly tied to the device's recombination operations. A lower recombination rate leads to a greater Voc, making this parameter dependent on material quality and junction integrity. It may be mathematically connected to the short-circuit current density and the saturation current density (J_o) using the equation [1]:

$$Voc = \left(\frac{nkT}{q}\right) \times \ln\left(\frac{Jsc}{j_o} + 1\right) \qquad (4.3)$$

High Jsc and Voc values are desired, but they do not influence overall device performance. The fill factor (FF) determines the form of the J-V curve and compares real power production to the theoretical maximum (Jsc × Voc). The maximum power point (MPP), where the product J×V is maximized, is used to compute it.

$$FF = \frac{(J_{mpp} \times V_{mpp})}{(Jsc \times Voc)} \qquad (4.3)$$

Series resistance lowers current flow, but shunt resistance generates leakage currents. Furthermore, flaws in material qualities or connections might impair optimal diode functioning. A high FF indicates that the solar cell transfers the available electricity efficiently and with little losses.

All three parameters (Jsc, Voc, and FF) define the most critical performance metric: the power conversion efficiency (η) shown in figure 4.3. The efficiency represents the fraction of incident solar energy successfully converted into electrical power. It is computed using the following equation:

$$\eta = \frac{(jsc \times Voc \times FF)}{p_{in}} \qquad (4.4)$$

where P_{in} is the incident light power density, typically 1000 W/m² under standard test conditions (AM1.5G spectrum).

Another parameter, that helps to indicate how good a solar cell is converting light into electricity is quantum efficiency. The quantum efficiency (QE) is the ratio of carriers collected by a solar cell to the number of photons of a given energy that impact the cell, and it can be expressed as a function of wavelength or energy. QE measurements or solar cells can be considered as: 1) External Quantum Efficiency (EQE), which includes the effects of optical losses such as transmission through the cell or reflection of light. 2) Internal Quantum Efficiency (IQE), which considers only the portion of light that is able to generate carriers.

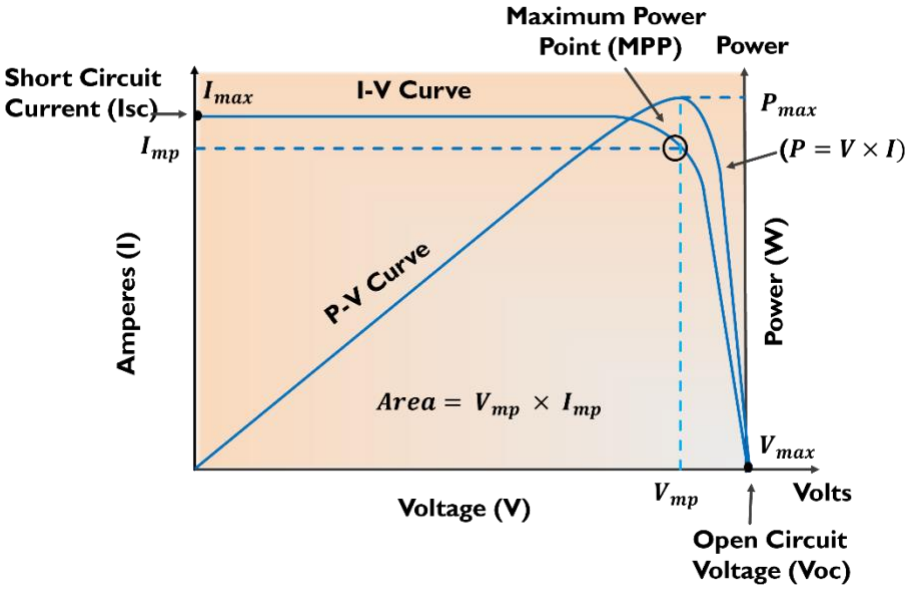

Figure 4.3: Solar cell I-V characteristics, showing operating point

4.3 External Quantum Efficiency

The external quantum efficiency (EQE) of a photovoltaic device is a spectrally dependent parameter that quantifies the effectiveness of converting incident photons into charge carriers. EQE reflects the possibility that a photon of a certain wavelength will gather a photogenerated electron at the device's electrical connections. This makes EQE an important technique for evaluating the spectrum performance of solar cells.

The short-circuit current density (Jsc) is calculated by integrating the product of the EQE and the incident illumination's spectral photon flux throughout the relevant wavelength range. Assuming

the device operates under linear response conditions and that the photocurrent generation is independent of the intensity of the incident radiation, Jsc is given by:

$$J_{sc} = q \int_{\lambda^1}^{\lambda^2} EQE(\lambda)\phi_{sun}(\lambda)d\lambda \qquad (4.5)$$

where q is the elementary charge (approximately 1.602×10^{-19} C), $\phi_{sun}(\lambda)$ denotes the spectral photon flux density of the standard AM1.5G solar spectrum (normalized to an irradiance of 1000 W/m²), and λ is the wavelength of the incident light.

Solar cell materials absorb photons of varying energies depending on the photon's wavelength. The ideal solar cell has an EQE in the square Short-wavelength photons (like ultraviolet light) carry more energy and are usually absorbed near the surface of the semiconductor. Their high energy allows them to quickly excite electrons, creating charge carriers (electrons and holes).

In contrast, long-wavelength photons (such as infrared and near-infrared light) have lower energy and can travel deeper into the solar cell before being absorbed. These photons create charge carriers in the device's deeper areas, where carrier collection may be less effective due to material quality and design.

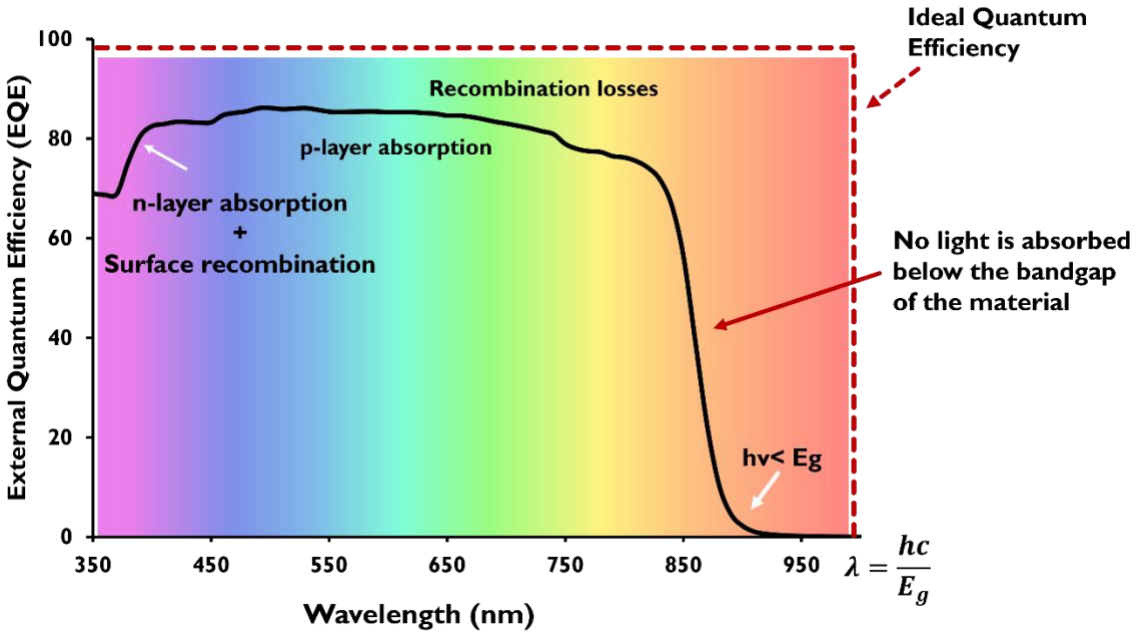

Figure 4.4: EQE spectrum regions correspond to different structural layers in a thin-film solar cells.

Photons of medium wavelengths, generally in the visible range, are frequently absorbed in the depletion zone of the p-n junction. The built-in electric field in this area effectively separates the

created electron-hole pairs and drives them toward the electrodes via drift, so contributing significantly to photocurrent. As a result, absorption in this region tends to yield higher charge collection efficiency as shown in figure (4.4).

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Chapter 5

Cadmium Telluride as a Photovoltaic Material

The previous chapter outlined general semiconductor physics, this chapter focuses on a specific material system: Cadmium Telluride (CdTe cadmium telluride (CdTe) technology, which is presently the thin-film technology with the lowest demonstrated cost per watt. CdTe is a II-VI semiconductor with a good mix of electrical, optical, and material characteristics that make it ideal for high-efficiency and cost-effective solar energy conversion.

This chapter details the structural and optical properties of CdTe, along with the specific fabrication techniques, such as Close-Spaced Sublimation (CSS) and Thermal Evaporation (TE), used in this work. Furthermore, it describes the device configuration, specifically the superstrate configuration that we used as the foundation for the experimental optimizations performed in the subsequent chapters.

5.1 Structural Properties

CdTe thin films generally crystallize in a zinc blende cubic structure [1], [2], which is ideal for photovoltaic applications. Cd^{2+} is bonded to four equivalent Te^{2-} atoms to form corner-sharing $CdTe_4$ tetrahedra. Te^{2-} is bonded to four equivalent Cd^{2+} atoms [2] to form corner-sharing $TeCd_4$ tetrahedra as shown in figure (5.1)

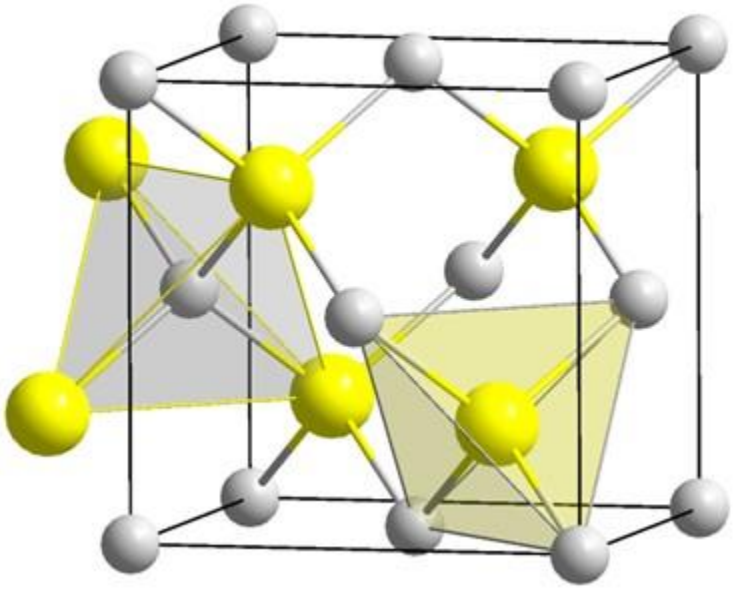

Figure 5.1: Crystal structure of CdTe from Wikipedia

CdTe can be n-doped by substituting the II-valence electron atom Cd with a III-valence electron atom, such as aluminum, gallium, or indium. n-doping can also be performed by substituting a VI-valence tellurium atom with an VII-valence electron element such as fluorine, chlorine, bromine, or iodine. The III and VII-valence atoms function as shallow donors [3]. Also, a tellurium vacancy functions as a donor [4] though its stability and energy level can vary depending on the growth conditions. CdTe can be p-doped by substituting Cd with an I-valence electron atom, such as copper, silver, or gold [3]. It is also possible to replace Te atoms with elements possessing V-valence electrons, such as nitrogen, phosphorus, or arsenic [5]. These elements function as shallow acceptors. But also, a Cd vacancy acts as an acceptor. In solar cells, p-doped CdTe is used. However, it is difficult to obtain CdTe with a high doping level [6].

However, depending on the growth process, minor quantities of the hexagonal phase may occur, affecting device performance. One crucial issue is grain size. Larger grains, generally more than 1 micrometer, assist to limit the number of grain borders where charge carriers can recombine, hence enhancing charge transport and efficiency.

Another important aspect is the crystallographic orientation of the CdTe film. Films with a (111) orientation are often preferred because they provide better lattice matching and epitaxy when combined with specific buffer layers, such as CdSe or CdSe [7]. Alloying the CdTe to mix with the buffer layer to form a graded absorber layer can reduce the band-gap to the lower band gap due to the bowing effect. Thus, band-gap engineering geared to controlling the composition profiles and spatial distribution of the CdSe content in the absorber layer can lead to enhance the overall performance of the cells [8], [9].

Defects and impurities in the CdTe layer, such as dislocations, interstitial atoms, and vacancies can operate as recombination sites, reducing carrier lifetime and limiting the solar cell's open-circuit voltage (Voc). $CdCl_2$ activation is a popular post-deposition therapy that mitigates these effects. This technique increases crystallization quality, minimizes defects, and enhances grain development, resulting in improved electrical characteristics for the CdTe absorber.

5.2 Optical Properties

CdTe thin films exhibit several key optical properties that make them highly suitable for photovoltaic applications.

A key feature of CdTe is its direct band gap of approximately 1.45 eV, which is nearly ideal for single-junction solar cells operating under the standard solar spectrum (AM1.5). This band gap enables CdTe to absorb a significant portion of the visible solar spectrum (figure 5.2) leading to efficient photon-to-electron conversion and reduced thermalization losses. Unlike indirect band gap materials (e.g., silicon), direct band gap semiconductors such as CdTe require significantly thinner absorber layers to successfully collect sunlight.

CdTe has a high absorption coefficient (>10^5 cm^{-1}) at photon energies over the band gap. This means that over 90% of incoming sunlight may be absorbed in a few microns of material, generally within a thickness range of 2-8 µm. This thin-film nature reduces raw material use and energy needs during manufacture, which is particularly advantageous for scalable, low-cost solar module production.

CdTe is chemically and thermally stable, compatible with various deposition techniques (such as close-spaced sublimation, vapor transport deposition, and sputtering), and well-suited for roll-to-roll or large-area module fabrication. Its abundance, relatively low toxicity, and established supply chain have contributed to its widespread adoption in utility-scale photovoltaic projects.

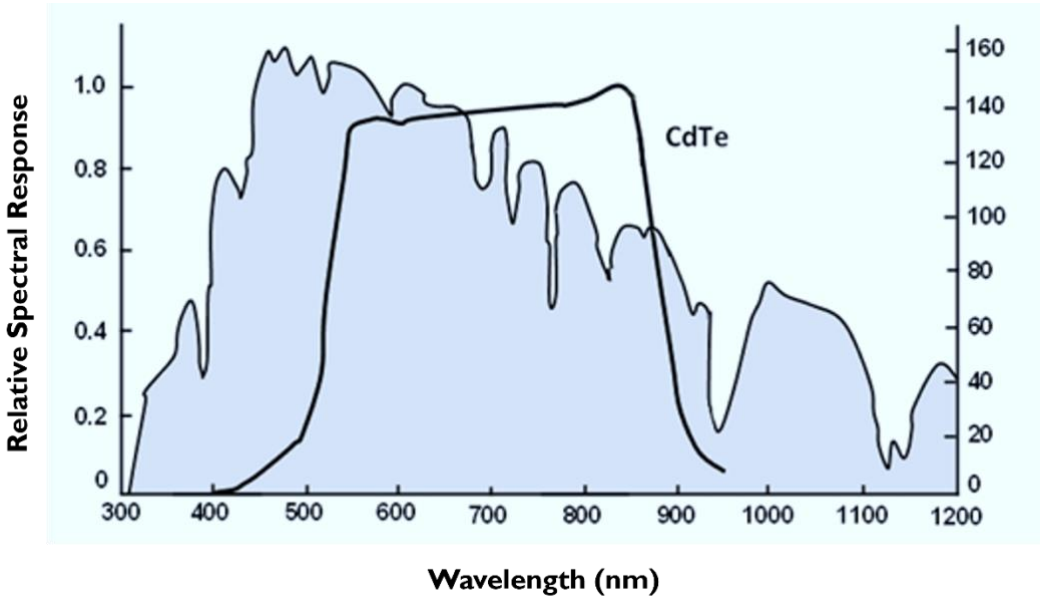

Figure 5.2: Solar irradiance spectra and spectral response of CdTe images from [9]

5.3 Solar Cell Device Structure

Until now, we have discussed the photovoltaic effect, the requirements for the material properties to come close to a perfect solar cell, and the possible geometries to separate and extract charge carriers.

Thin-film solar cells are usually more complex devices with a higher number of layers that are optimized for one or several purposes. In general, there are two configurations possible for any thin-film solar cell as shown in Figure 5.3. The first possibility is that light enters the device through a transparent superstrate.

The superstrate has to maintain the mechanical stability of the device while at the same time being extremely transparent. The superstrate is followed by layers which are part of the front contact, followed by the absorber layer and the layers that form the back contact. The second possibility is to inverse the layer stack, starting with the front contact, the absorber, and the back contact. These layers are all deposited on top of a substrate. Because light does not have to pass the substrate to enter the solar cell, the substrate can be transparent or opaque.

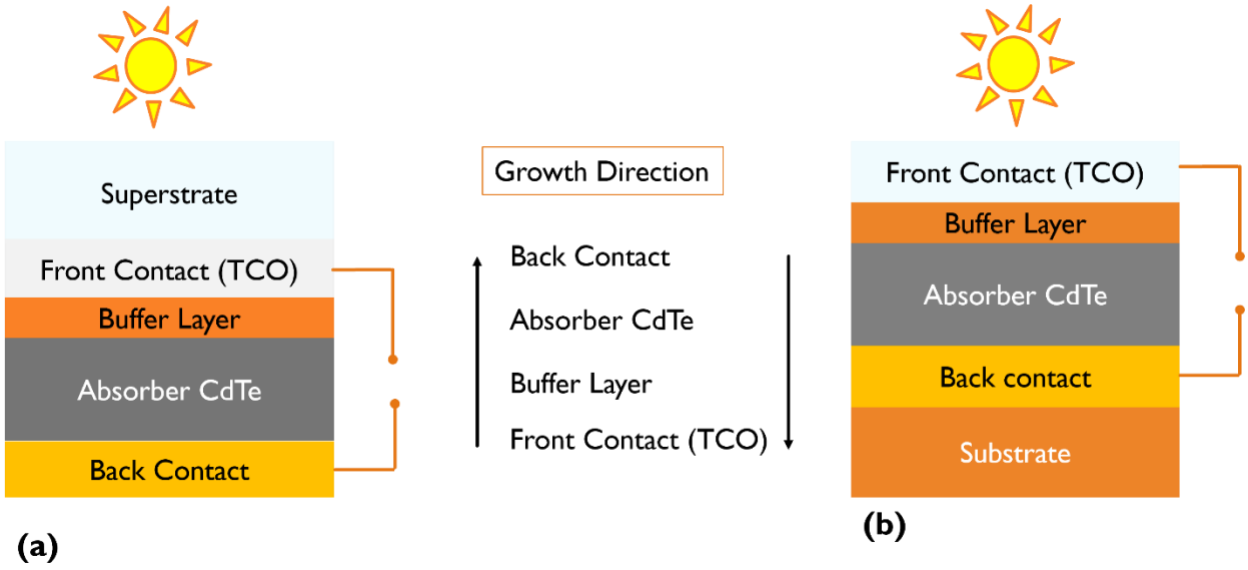

Figure 5.3: Sketch of the layer sequences to fabricate the system for CdTe thin-film solar cells (a) Superstate configuration (b) Substrate configuration

5.3.1 Transparent Conducting Oxide (TCO)

This layer plays a dual role: It must be sufficiently transparent to allow sunlight to reach the absorber layer while also being conductive enough to collect and transport photogenerated electrons toward the external circuit. TCO layers are often deposited on glass substrates, which serve as the mechanical support for the device.

The three most widely applied transparent conducting oxides (TCOs) are fluorine-doped tin oxide (SnO_2: F), aluminum-doped zinc oxide (ZAO) and indium tin oxide (ITO). Similar to glass substrates, TCO thin films must withstand high processing temperatures and exhibit strong chemical stability. In addition, suitable TCOs should meet the following criteria:

- Wide bandgap (Eg > 4 eV).
- Optical transmittance in the range of 80–90%.
- Sheet resistance of about 5 Ω/cm^2.

For CdTe-based solar cells, the most frequently employed TCOs are SnO_2: F, ITO, Cd_2SnO_4, and (ZAO). ITO offers an excellent balance of optical transparency and electrical conductivity, but its use is limited by the low natural abundance of indium (roughly 0.05 ppm in the Earth's crust). On the other hand, SnO_2: F is more widely adopted because tin is relatively abundant and the material maintains superior chemical and mechanical stability at elevated temperatures.

The essential properties of an effective TCO can be summarized as:

- High optical transparency.
- Low electrical sheet resistance.
- High surface uniformity, with minimal roughness and few pinholes.

Both transparency and sheet resistance vary inversely with film thickness. To evaluate and optimize TCO performance with respect to thickness, the Haacke figure of merit [10] is often used:

$$\boldsymbol{F.M = \frac{(T_{ave})^{10}}{R_{sh}}} \qquad (\mathbf{5.1})$$

where T_{ave} is the average transmittance and R_{sh} is the sheet resistance.

5.3.2 CdTe Absorber Layer

The most important material of the solar cells is the active or absorbing material and the p part of the heterojunction. It is responsible for absorbing photons and generating electron-hole pairs. The photogenerated electrons and holes must be separated and directed toward their respective electrodes to generate electric current upon light absorption.

The research on CdTe-based photovoltaics has historically explored several cell structures, including p-i-n junctions, Schottky barriers, and homojunctions. However, the heterojunction design emerged as the most effective and widely adopted structure, while various wide-bandgap semiconductors can serve as the n-type partner for CdTe which naturally exhibits p-type characteristics when deposited at temperatures exceeding 570K. This effectiveness stems from the beneficial intermixing between CdSe and CdTe, which reduces native defects and creates an interface that functions similarly to a homojunction.

CdTe thin films are fabricated using a diverse range of techniques, generally categorized into high-temperature Close-Spaced Sublimation (CSS) and low temperature Thermal Evaporation (TE) techniques (used in this thesis). They are the primary methods used for laboratory and industrial scale production of high-efficiency modules, which currently achieve efficiencies over 20% in the commercial market. These industrial processes yield high-efficiency modules, which currently achieve efficiencies of approximately 19% to 19.7% in the commercial market, with laboratory cell records exceeding 22%.

A significant advantage of the CSS method is the production of high-quality films with large, columnar crystalline grains (typically 5–10 µm). These large grains are beneficial because they minimize transverse grain boundaries, which can otherwise impede charge carrier lifetime and movement. However, optimizing film thickness presents a technical challenge. CdTe has an absorption coefficient of about 10^4 cm^{-1} with 90% of the photons absorbed in 1 µm of the film [11].

In practice, CSS-deposited films should be much thicker (around 7–8 µm) to prevent the formation of pinholes and voids that occur as grain size increases. Excessive thickness can be detrimental, in a 10 µm thick film, only the smart part near the junction actively contributes to light conversion. The remaining inactive material increases series resistance, which can lower overall cell efficiency [12].

Among low-temperature techniques, TE is significant for its specific film characteristics. TE typically produces compact CdTe films and a small average grain size of 0.1–0.5 µm. The smaller grain size inherent to this method can lead to low charge carrier mobility and short lifetimes, which initially limits the efficiency of the p-n junction and the collection of photo-generated carriers. To overcome these limitations, a post-deposition annealing known as activation treatment is applied. This process enhances grain growth, reduces the density of misfit dislocations and stacking faults, and optimizes grain boundaries [12,13]. Through these thermal-chemical treatments, the grain size is increased sufficiently for the CdTe layer to serve as an effective absorber in high-efficiency solar cells. Despite the differences in initial film properties between various techniques, these post-deposition steps allow CdTe-based cells to achieve high performance relatively independently of the chosen deposition method [14].

5.3.2.1 The Activation Treatment

Establishing a high-efficiency CdTe solar cell requires a critical activation step known as the chlorine treatment. This post-deposition process, typically performed in a chlorine-containing atmosphere at temperatures between 350 °C and 450 °C, is essential for transforming the as-deposited layers into a high-quality absorber. Without this treatment, CdTe films often suffer from small grain sizes, high resistivity, and significant structural defects that limit solar-to-electric conversion efficiency to only around 1–5% [15].

The treatment promotes a significant increase in grain size, which reduces the overall density of grain boundaries. For films deposited at low temperatures, grain growth can enlarge crystals up to five times their original size. Chlorine acts to deactivate electron traps at grain boundaries through passivation, which drastically reduces recombination centers and improves minority carrier lifetimes. The treatment facilitates the interdiffusion of cadmium selenide (CdSe) and CdTe at their interface which helps to reducing lattice mismatch [16].

5.3.3 Back Contact

A metallic back contact is applied on the opposite side of the CdTe absorber. Materials such as copper/gold (Cu/Au), molybdenum (Mo), or carbon-based pastes are commonly used. The rear contact collects holes and facilitates their flow into the external circuit. A well-designed back contact is critical for lowering series resistance and preventing carrier recombination at the interface, which can diminish the device's fill factor and overall efficiency.

The CdSe-CdTe interface, which forms a heterojunction, is critical to device functioning. The built-in electric field at this junction aids charge separation. It lowers photogenerated carrier recombination, increasing the open-circuit voltage (Voc) and short-circuit current density (Jsc). Furthermore, appropriate band alignment guarantees that carriers move efficiently across the junction while reducing energy losses.

CdTe is a promising option for thin-film solar cells due to its perfect band gap, high absorption coefficient, effective charge separation at the heterojunction, and the promise for low-cost, large-scale manufacture. Its proven performance in commercial photovoltaic modules and utility-scale installations further underscores its significance as a central material in developing sustainable solar energy technologies.

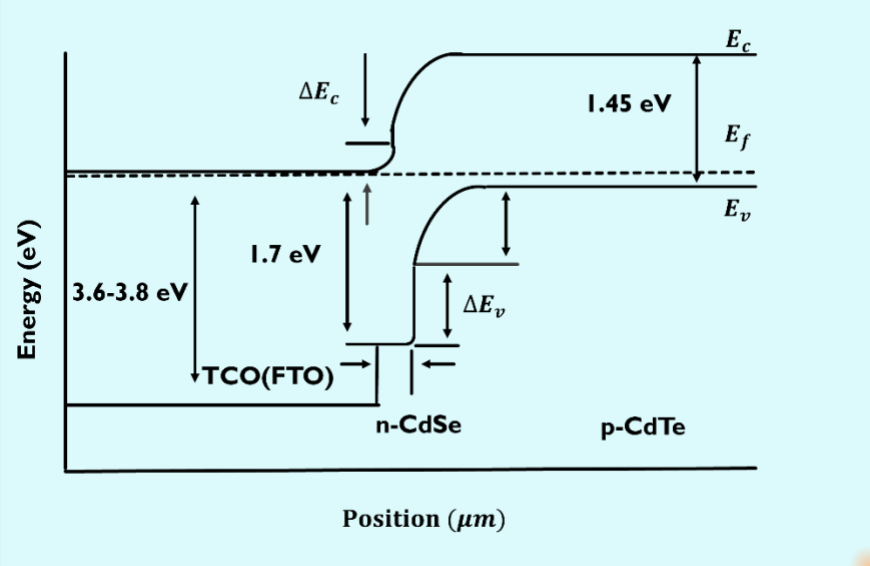

Figure 5.4: Band diagram of TCO/CdSe/CdTe cell image from [9]

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Chapter 6

Growth Techniques of Thin Films

(used in this thesis)

The performance and reliability of solar cells are strongly influenced by the method used to deposit the thin film layers. Each deposition technique affects the crystal structure, defect density, grain size, and interface quality of the thin film, thereby impacting key device parameters such as efficiency and reproducibility. Various deposition methods have been developed to fabricate high-quality thin films on various substrates. Each with its trade-offs between film quality, process complexity, and scalability. Below are shown and described the growth techniques that we used during our work for thin films depositions.

6.1 Close-Spaced Sublimation (CSS)

Close-spaced sublimation (CSS) is a physical vapor deposition technique extensively used for fabricating CdTe solar cells. In this process, a CdTe source material and the substrate are positioned very close to each other typically from few millimeters to a few centimeters apart within a sealed chamber. CSS is almost exclusively performed in an inert atmosphere (Argon, Nitrogen, or Helium) mixed with a small amount of Oxygen. This background gas is essential because it moderates the transport of vapor species through diffusion, preventing the uncontrolled rapid evaporation that would occur in a vacuum. At elevated temperatures, the CdTe source sublimates, and the resulting vapor diffuses the short distance to the cooler substrate, where it condenses to form a compact polycrystalline thin film.

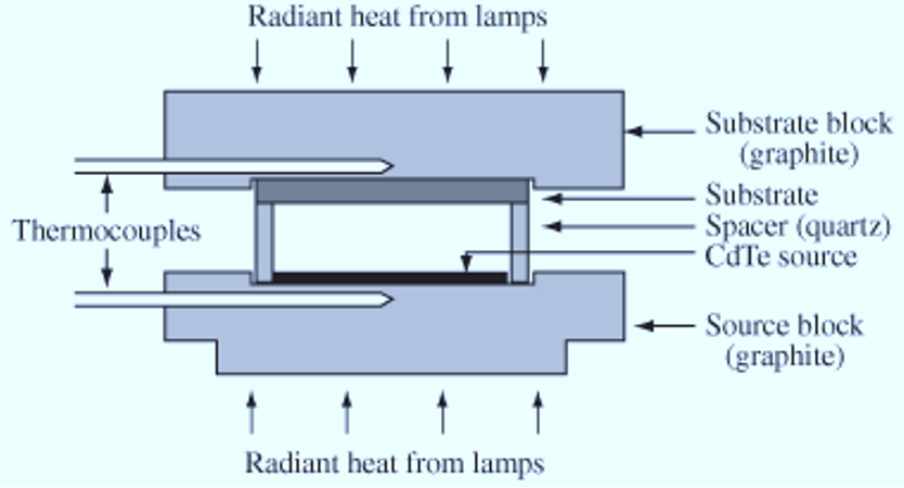

Figure 6.1: Schematic view of close-spaced sublimation (CSS) apparatus [1].

One of CSS's main benefits is its high deposition rate, which makes it ideal for large-scale industrial manufacturing. Furthermore, the approach supports good grain development and crystallinity in the resultant film, thanks to the high substrate temperature, which helps to improve electrical characteristics and photovoltaic performance. CSS is also compatible with inline production techniques, which enhances its commercial feasibility.

CSS, on the other hand, demands quite high substrate temperatures, approximately 500-600°C, which might limit substrate options and increase energy usage during production. Furthermore, maintaining exact control over the thickness and homogeneity of the deposited layer can be difficult, necessitating thorough calibration and process optimization to assure consistent results.

6.2 Thermal Evaporation

Thermal evaporation is a physical vapor deposition process used in both research and manufacturing settings. This method involves heating CdTe material in a crucible or boat within a high-vacuum chamber until it evaporates. The vapor rises and condenses onto a colder substrate, generating a thin coating. The deposition rate and film quality are affected by the source temperature, vacuum level, and deposition geometry.

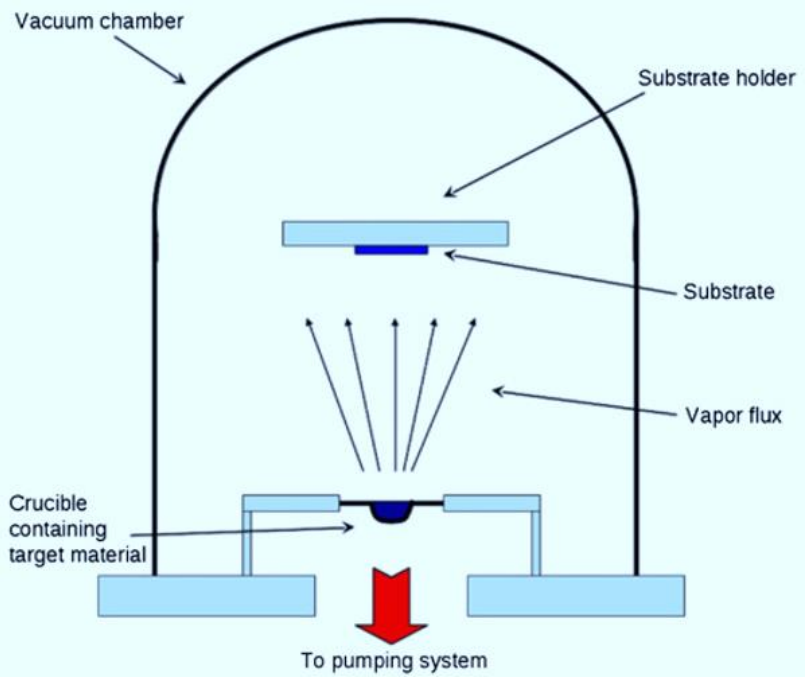

Figure 6.2: Schematic view of thermal evaporation apparatus [2].

The significant advantage of thermal evaporation is its relative simplicity. It enables precise thickness control and allows the deposition of highly pure films due to the high-vacuum

environment. This makes it suitable for experimental studies where reproducibility and material purity are essential. However, the technique typically results in smaller grain sizes unless followed by post-deposition annealing or recrystallization steps. Additionally, uniformity over large areas can be an issue due to the directional nature of vapor transport, although this can be mitigated through rotating substrates or multi-source configurations.

6.3 Sputtering

Sputtering is a physical vapor deposition (PVD) process in which atoms are ejected from a solid target material due to momentum transfer from energetic particles, typically ions from a plasma. An inert gas, such as argon, is put into a vacuum chamber and ionized by an applied electric field, resulting in a low-pressure plasma. Positive argon ions are propelled toward the negatively biased target (cathode) and collide with the target material's surface atoms. If the kinetic energy imparted during these collisions exceeds the surface binding energy of the target atoms, they are expelled. The expelled atoms move through the low-pressure gas phase with little collisions before condensing on a substrate to produce a thin film.

The sputtering yield (number of atoms ejected per incident ion) depends on several factors, including the ion energy, target atomic mass, angle of incidence, and surface binding energy. The process can be performed in different modes, such as direct current (DC) sputtering for conductive targets, radio frequency (RF) sputtering for insulating targets, both can be magnetron sputtering, this employs magnetic fields to confine electrons near the target, increasing plasma density and sputtering efficiency.

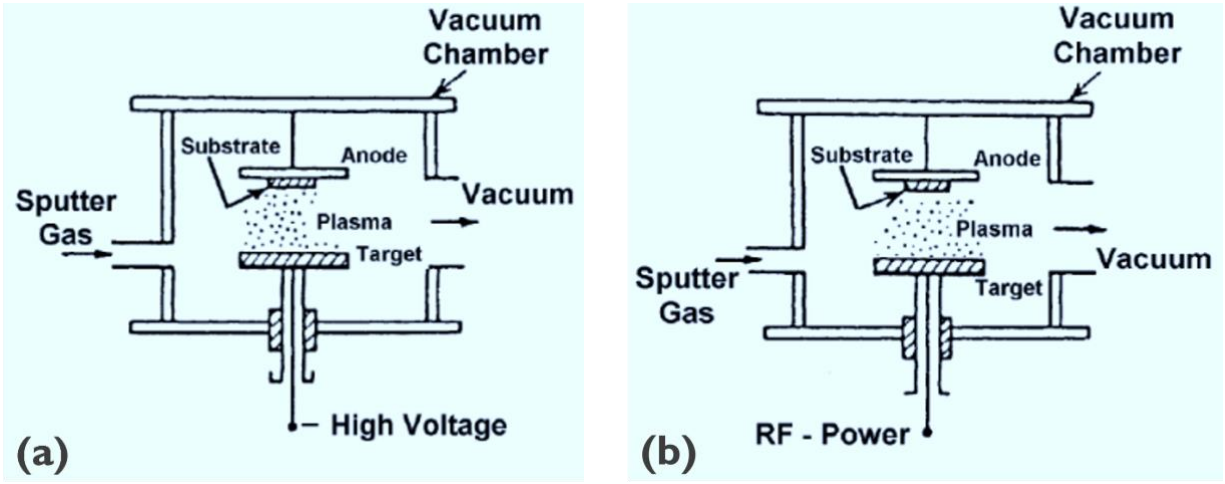

Figure 6.3: DC Diode (a) and RF Diode (b) [3].

6.4 Characterization Techniques

To assess the physical, optical and electrical properties and optimize device performance, several electrical and optical characterization techniques are employed:

6.4.1 X-Ray Diffraction (XRD)

X-ray diffraction (XRD) is a widely used non-destructive technique to investigate the structural properties of crystalline materials, particularly thin films and thin-film devices such as CdTe photovoltaics. It gives quantitative data on crystal structure, phase composition, crystallite size, strain, and defect density, making it crucial for thin-film solar cell characterization.

The approach relies on the elastic scattering of X-rays from periodic atomic planes in the crystal lattice. Constructive interference arises when the path difference between waves scattered from consecutive planes is an integer multiple of the X-ray wavelength, as described by Bragg's law:

$$\boldsymbol{n\lambda = 2dsin\theta} \qquad (\mathbf{6.1})$$

where n is an integer, λ is the wavelength of the incident X-rays, $d_{(hkl)}$ is the spacing between atomic planes with Miller indices (hkl), and ϑ is the diffraction angle. The recorded diffraction pattern is a structural fingerprint, revealing information on the crystalline phases present, their preferred orientations (texture), and the distribution of lattice spacing. Peak broadening also enables the estimate of crystallite size (by the Scherrer equation) and micro strain.

For thin-film investigation, modified powder diffraction geometries are frequently used, with the specimen tangential to the focusing circle between the incident beam and detector. In this setup, intensity maxima occur when the angle between the incident and diffracted beams meets the Bragg condition. The diffraction pattern as a function of 2θ includes two sorts of information:

1. **Peak positions** – corresponding to specific lattice plane spacings and enabling phase identification.
2. **Peak shapes (profiles)** – reflecting the distribution of d-spacings and thereby providing insight into strain, defects, or compositional variations within the film.

In typical XRD, both the source and detector move symmetrically, probing the whole film. However, for ultra-thin films like CdTe absorber layers, traditional XRD may lack surface sensitivity. In such instances, grazing incidence XRD (GIXRD) is used. The incident beam strikes the sample at shallow angles (0.5°-1°), limiting the depth of X-ray penetration and making the method very surface sensitive.

XRD is critical for determining crystallinity and texture, both of which have a substantial effect on device performance. Such orientation lowers recombination at grain borders while increasing charge carrier transit.

6.4.2 Scanning Electron Microscopy (SEM)

SEM investigations were conducted to analyze the surface morphology, grain size, and orientation of the sample materials. Figure 6.4 depicts a schematic diagram of the SEM. An electron gun is used to generate a monochromatic electron beam, which is then directed via the first condenser lens and condenser aperture. The aperture is used to remove some high-angle electrons.

The second condenser lens is used to provide a finely focused beam. The deflection coils scan the electron beam across the sample surface in a raster pattern. A vacuum is essential to prevent scattering and absorption by air molecules. When the focused electron beam strikes the sample surface, an interaction volume is generated where elastic and inelastic scattering occur. These interactions produce various signals, primarily Secondary Electrons (SE), which provide topographic information, and Backscattered Electrons (BSE), which provide compositional contrast. These signals are detected by appropriate detectors to form an image. The x-rays emitted from a sample can provide chemical information. An energy dispersive x-ray (EDX) spectrometer is made up of a solid-state x-ray detector installed inside the SEM chamber. It is typically built of lithium-drifted silicon, Si (Li), and includes signal processing devices. The Si (Li) detector converts emitted x-rays into an energy histogram. Each element's relative abundance and atomic composition can be calculated using a succession of peaks.

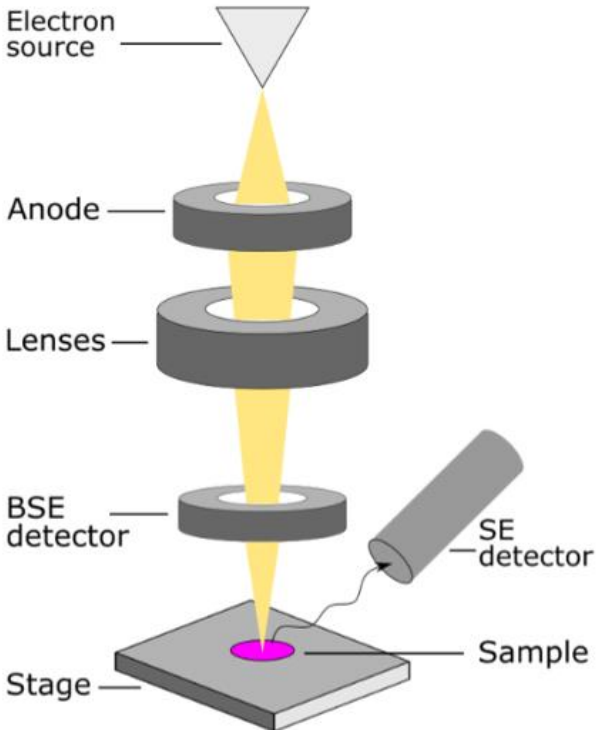

Figure 6.4: Schematic diagram of the SEM

6.4.3 Atomic Force Microscopy (AFM)

This technology, introduced in 1986 [58], is a powerful tool for surface analysis. It produces 2D and 3D images and can provide a true topographic representation of the sample via its vertical view. Figure 3.9 depicts a schematic diagram for a common AFM instrument. The probe consists of a microfabricated cantilever with a sharp tip placed on or below the sample surface. The computer-controlled piezoelectric actuator moves the sample with precision.

AFM can be operated in three modes: contact mode (true), non-contact mode, and intermittent (known as tapping) mode.

(a) Contact mode

A soft silicon nitride cantilever is commonly used to probe the surface. The tip is held at a constant height at or above the surface, and the cantilever deflection is employed to create an image.

(b) Non-contact mode

The tip oscillates at its resonant frequency at a small distance above the surface. The signal sent to the piezoelectric actuators required to maintain the resonance frequency is then used to create a topographic image.

(c) Intermittent mode

The cantilever is initially oscillated at its resonance frequency with substantially larger amplitudes than those used in non-contact mode. As the tip approaches the surface, it reduces its amplitude and makes contact. This is the primary way of imaging when atomic resolution is not required.

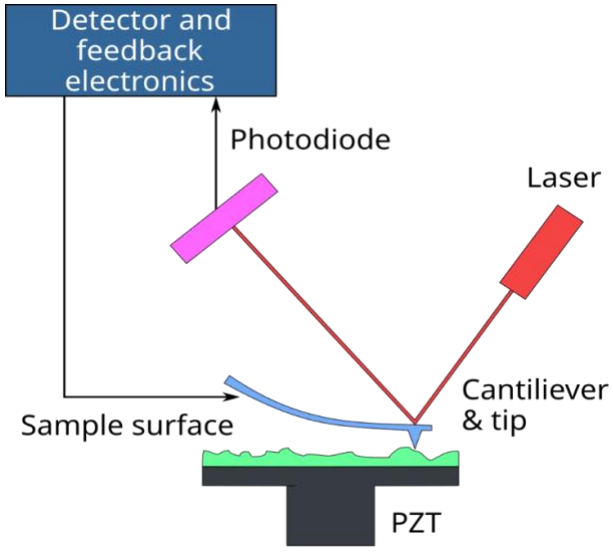

Figure 6.5: Schematic diagram for a common AFM instrument from Wikipedia

6.4.4 Raman Spectroscopy

Raman spectroscopy is a method that uses a material's distinctive spectral pattern, or fingerprints, to detect and offer information about chemical structures and physical forms. In 1928, Raman and Krishnan [4] first experimentally observed the phenomenon of inelastic scattering of light after it was postulated by Smekal [5] in 1923. Later on, this phenomenon was named as Raman spectroscopy.

Raman spectroscopy uses inelastic scattering of monochromatic light from a laser in visible, near infrared, or near UV ranges. When light interacts with phonons or other excitations in the system, the energy of the incident photon changes. A Raman spectrometer's schematic diagram is shown in Figure 6.6.

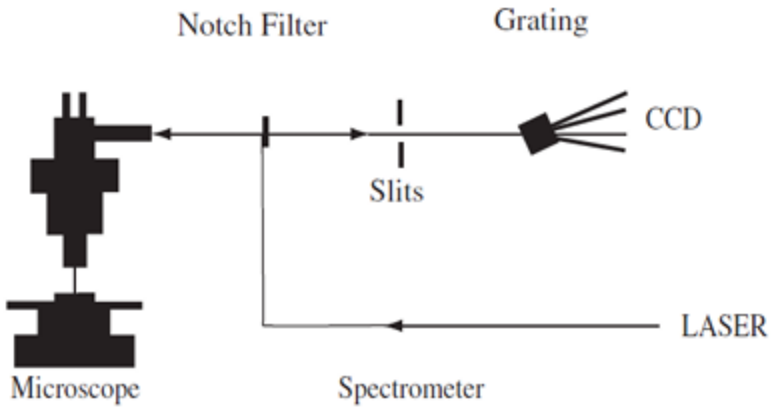

Figure 6.6: Schematic diagram of a Raman spectrometer instrument [6]

A pinhole is used to concentrate a laser, which is then collected as an enlarged parallel beam. The laser directed via a pinhole is collected by the beam. For the radiation that acts as an interference filter, a notch filter is employed. After the light enters the monochromator, it is detected by the charged coupled device (CCD) detector. The majority of vibrations have wavenumbers between 50 and 1800 cm^{-1}, whereas certain molecular vibrations have wavenumbers as high as 3500 cm^{-1}. Line widths range from 1 to 5cm^{-1}**.**

6.5 References

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Chapter 7

Study of CdSeTe/CdTe devices (2µm)

7.1 Introduction

The primary goal of this chapter is to describe the fabrication of high-efficiency CdSeTe/CdTe devices fabricated via thermal evaporation, optimized during my PhD thesis. The Se-Te intermixing study was the first step in my PhD work for optimizing the fabrication of $CdSe_xTe_{1-x}$/CdTe devices with an absorber thickness of 2 µm. This provided a reliable starting point for further study of the development of the absorber and the optimization of the devices.

Devices were fabricated at low substrate temperatures by thermal evaporation. We deposit CdSe and a thin layer of CdTe followed by vacuum annealing at 450°C to encourage selenium-tellurium intermixing to create a $CdSe_xTe_{1-x}$ alloy. Subsequently, a 1.4 µm thick CdTe layer is deposited.

Structural and optoelectronic investigations (XRD, Raman, SIMS, and EQE analysis) show that vacuum annealing reduces Te interstitial defects, improves crystal quality, and increases minority carrier lifetime.

7.2 Materials and methods

A Horiba Jobin-Yvon LabRam HR800 microprobe setup (in backscattering geometry) is used for measuring Raman spectra using an exciting light at 532 nm (He–Ne laser).

XRD is used to analyze the crystalline structure using a Philips vertical diffractometer equipped with a Goebel monochromator and Cu-Kα radiation.

A Cs+ primary ion beam at a 10 kV accelerating voltage (or 5.5 keV impact energy) and the detection of positive secondary ions were used for SIMS depth profiles on a CAMECA IMS-4f.

An HP4284A LCR performs CV, DLCP, and AS. A Janis cryostat with a Lakeshore 325 temperature controller controls the temperature between 90 and 330 K in a vacuum of 10^{-4} Pa. 100 kHz and 1 MHz bias frequencies were used for DLCP.

A commercial LOANA solar cell analysis equipment is used to measure the external quantum efficiency (EQE), which is then calibrated using a silicon reference sample with a known EQE and an incident spotlight measuring 1 mm by 2 mm.

A Keithley Source Meter 2420 is used to measure current density-voltage (JV) characteristics under an AM 1.5 spectrum at 100 mW/cm2 using a LOT Quantum Design Europe solar simulator LS0306.

7.3 Device fabrication

The superstrate arrangement of $CdSe_xTe_{1-x}$/CdTe devices are fabricated by low substrate temperature deposition. The front contact is made of a commercial transparent conductive oxide (TCO) that is supplied by NSG (Nippon Sheet Glass) Pilkington, TEC C12D.

1) Standard Device (Stan-D) without Vacuum annealing: 300 nm thick CdSe was deposited on the TCO and ffollowing with a 1.7 µm thick CdTe were deposited both by vacuum evaporation (VE) at a substrate temperature of 340 °C.

2) Vacuum Annealing Device (Vac-Ann): 300 nm thick CdSe layer is followed by 300 nm thick CdTe layer were deposited by VE at 340 °C, followed by vacuum annealing at 450 °C to form $CdSe_xTe_{1-x}$ alloy. Subsequently, a 1.4 µm thick CdTe layer is deposited with the same procedure

Subsequently, a $CdCl_2$-methanol solution is drop-cast onto the surface and then annealed in air at 390 ^oC to activate the absorber. The CdSe/CdTe layers are also mixed by the $CdCl_2$ treatment, which creates the desired $CdSe_xTe_{1-x}$ compound in the direction of the junction. In order to increase cell stability, the samples are finally etched in a Br-MeOH solution, which eliminates the $CdCl_2$ residues from the surface while also creating a Te-rich surface that encourages the production of CuxTe at the CdTe/back contact junction [3]. To create the back contact, a 0.5 nm thick copper and a 30 nm thick gold layer are deposited using vacuum evaporation. Lastly, to diffuse Cu into the absorber, the device is air-annealed at 200 °C.

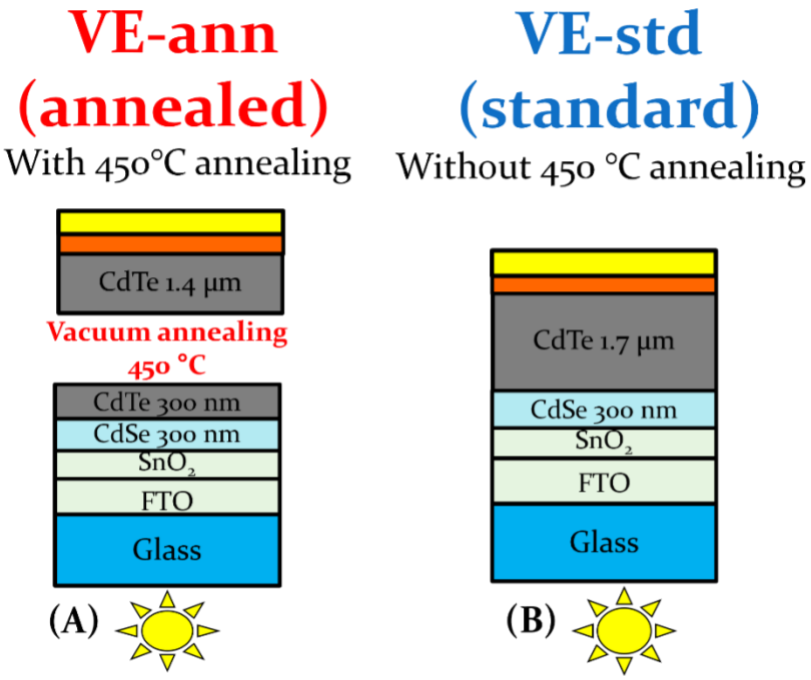

Figure 7.1: Device configuration of (A) Vacuum Anneal Stack and (B) Standard Stack.

7.4 Result and Discussion

In this work, we investigated the effect of vacuum annealing on the CdSe/CdTe stack by performing XRD measurements on both the as-deposited absorbers and those subjected to vacuum annealing.

7.4.1 Absorber Study

In the as-deposited sample, a strong diffraction peak is observed at 23.6°, corresponding to the [111] orientation of CdTe, along with a weaker peak at 25.3°, associated with the [002] orientation of CdSe (Figure 7.2). The difference in peak intensity arises because the top CdTe layer partially shields the underlying CdSe layer.

With vacuum annealing at 450 °C, the XRD spectra reveal significant modifications in the film structure. The CdTe [111] peak shifts toward higher diffraction angles, indicating a larger incorporation of Se into the CdTe lattice [4]. Simultaneously, the CdSe [002] peak exhibits an increase in intensity, suggesting that the CdSe phase becomes more prominent near the surface after annealing.

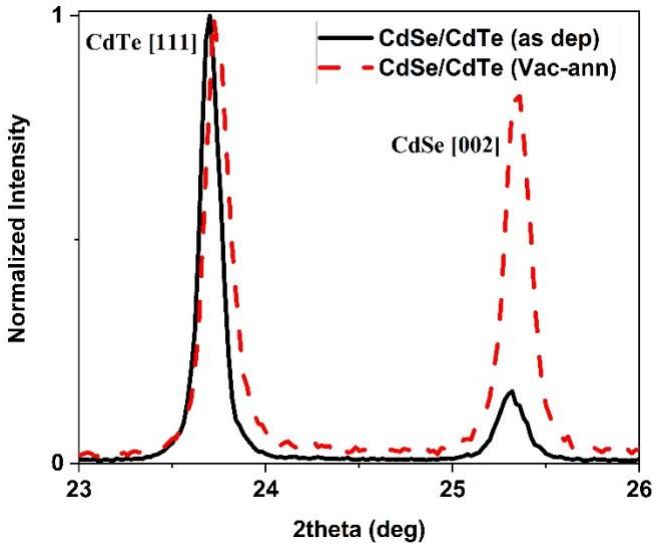

Figure 7.2: XRD patterns of the 300 nm CdSe/300 nm CdTe stack: 1) as-deposited and 2) Vac-Ann sample (vacuum annealing at 450 °C)

Raman analysis (figure 7.3) further highlights the effect of annealing on the surface composition. In the as-deposited case, the peak at 125 cm^{-1} is attributed to the vibrations of elemental Te,

while the peak at 141 cm^{-1} originates from the overlap of the transverse optical (TO) phonon modes of CdTe and elemental Te. A third, weaker peak at 165 cm^{-1} corresponds to the longitudinal optical (LO) phonon mode of CdTe.

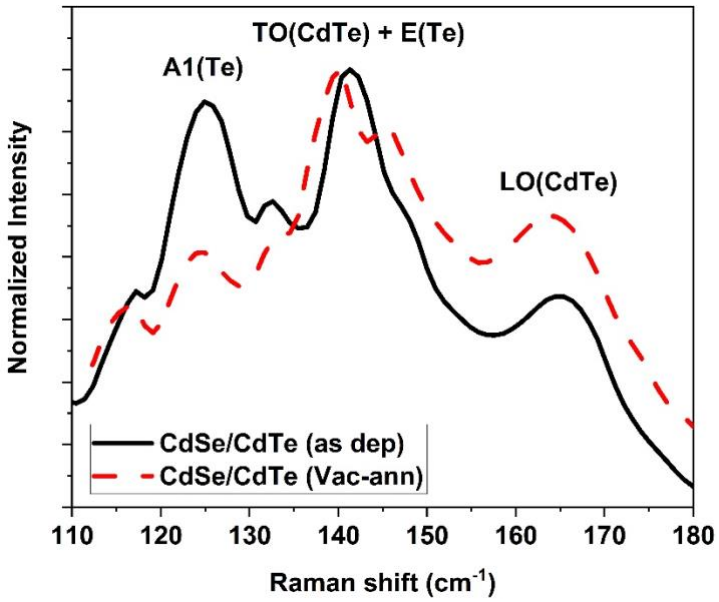

Figure 7.3: Raman spectra of As-deposited and Vacuum ann

After annealing, a pronounced reduction of the A1(Te) peak is observed, indicating a significant decrease in elemental Te at the surface. This reduction suggests that Te either recombines into the absorber matrix or diffuses toward the bulk. At the same time, the LO(CdTe) peak becomes more intense and shifts to 164 cm^{-1}, pointing to an improvement in CdTe lattice quality as well as a partial release of compressive stress [5]. For the same reason, the TO(CdTe) mode shifts toward lower wavenumbers, causing the 141 cm^{-1} feature to split into two distinct peaks [6].

However, the relative intensity of these TO peaks cannot be accurately assessed due to the ambiguity of the signal in the as-deposited sample.

Taken together, the XRD and Raman results indicate that vacuum annealing promotes interdiffusion of Se and Te within the CdSe/CdTe stack, leading to alloying and compositional mixing of the absorber layers.

Selenium incorporation and its distribution within the absorber are key factors influencing device performance. Secondary ion mass spectrometry (SIMS) provides a qualitative assessment of the Se content in the crystal structure. Since Se and Te are antagonistic in compound formation, the Se distribution was evaluated relative to the Te signal.

Figure 7.4 shows the depth profile of the Se/Te ratio (in logarithmic scale), where the abscissa corresponds to the depth from the absorber surface to the TCO. The vacuum-evaporated (VE) annealed devices exhibit the highest Se/Te ratio near the CdSeTe/TCO junction.

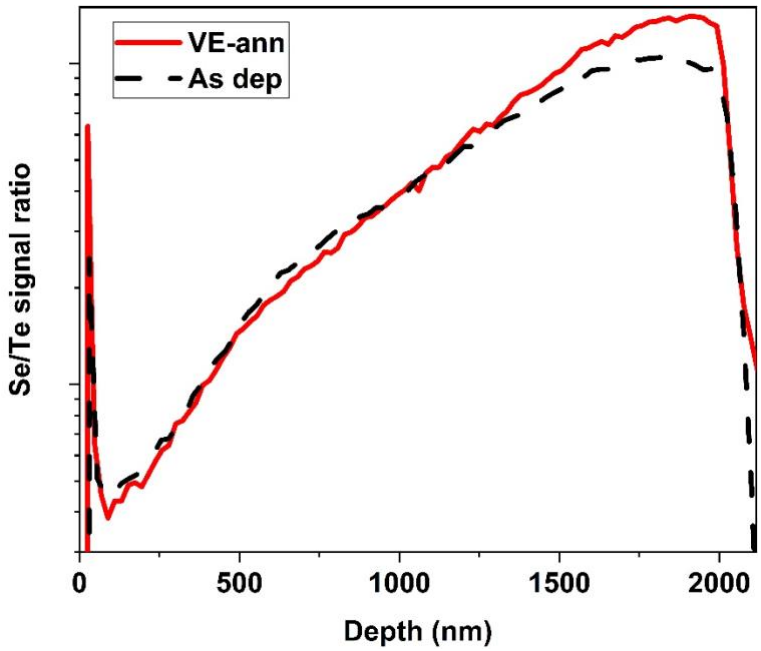

Figure 7.4: SIMS depth profiles showing selenium distribution through the absorber normalized on Te signals (in logarithmic scale) for as deposited and vacuum anneal device.

This observation is consistent with the Raman results, which indicated a reduced presence of Te in Vacuum Annealed samples. In the back-contact region, both sample vacuum anneals and as deposited samples show a similar Se/Te profile.

7.5 Performance of Devices

The External Quantum Efficiency (EQE) profiles demonstrate a significant enhancement across the entire spectral range for the VE-ann sample compared to the VE-std case. This substantial reduction in EQE response for the VE-std device can be attributed to two potential mechanisms:

1). It is possible that a thin, unmixed CdSe layer remains at the junction, contributing to parasitic absorption, as previously observed by Paudel et al. [7]. This hypothesis is partially supported by the X-ray diffraction (XRD) data (Figure 7.2), which shows a smaller peak shift for the VE-std sample, indicating limited Se diffusion into the bulk compared to the annealed sample. However, this explanation contradicts the Secondary Ion Mass Spectrometry (SIMS) data, which would be

expected to show a higher Se/Te signal ratio at the junction if a distinct CdSe layer were still present.

2). A more likely explanation is a higher rate of carrier recombination within the VE-std absorber. Conversely, the improved performance of the VE-ann sample suggests a reduction in recombination centers, leading to an increased diffusion length for photo-generated carriers, or potentially an expansion of the depletion region width [8].

Overall, the EQE analysis strongly indicates that the VE-ann process effectively reduces the defect density within the absorber material, thereby improving charge collection efficiency.

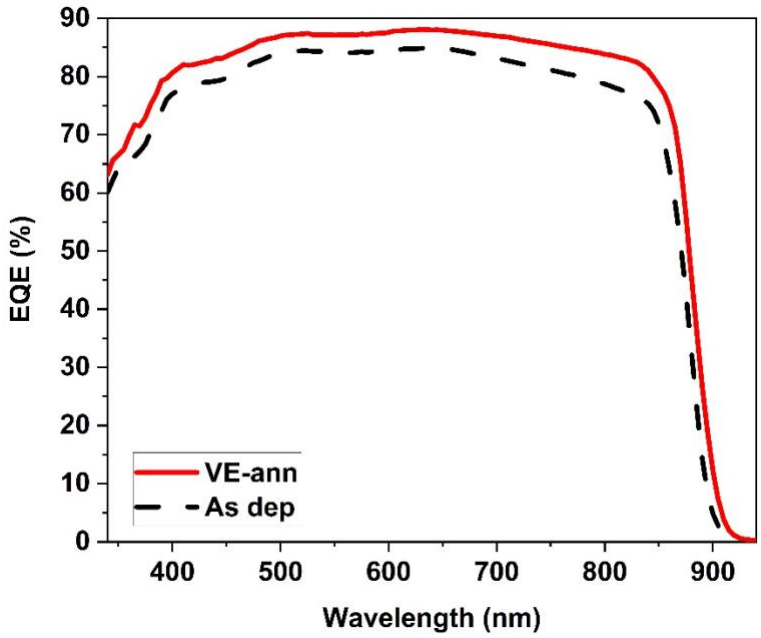

Figure 7.5: Comparison of EQE of as deposited and VE-Ann devices.

The band gap energy of the absorber was determined from the wavelength corresponding to the maximum negative derivative of the EQE curve at long wavelengths (Figure 7.5) [9]. The band gap energy (E_g) was calculated using the relationship:

$$E_g[eV] = \frac{1240}{\lambda_{peak}[nm]} \qquad (7.1)$$

The extracted values are (shown in the figure 7.6) 1.40 eV for the VE-Ann case, and 1.41 eV for as deposited devices. The slightly narrower band gap observed in the VE-Ann sample can be attributed to the higher Se concentration at the junction, as discussed earlier, which extends the absorption spectrum toward longer wavelengths. Overall, all preparation methods demonstrate the desired band gap reduction, confirming the bowing effect of selenium incorporation.

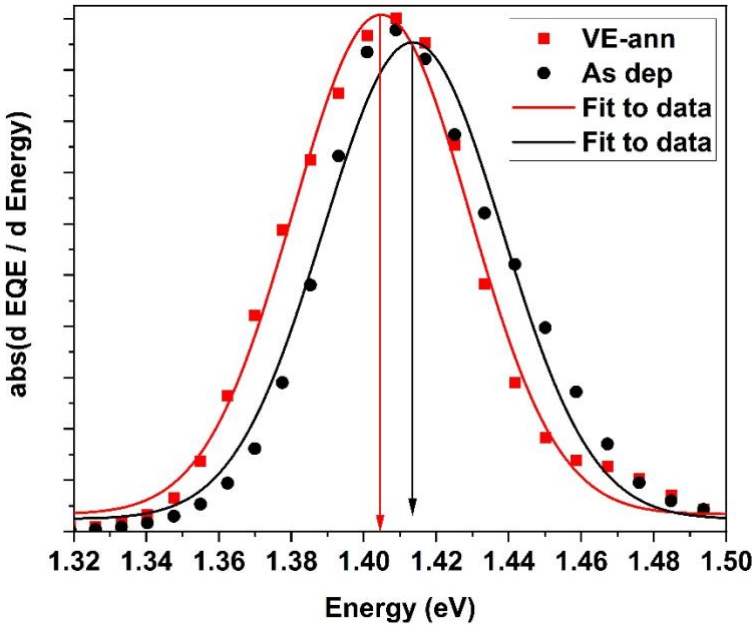

Figure 7.6: Band gap energy of the absorbers near the junction calculated from the EQE

Figure 7.7 compares the current density-voltage (J-V) characteristics of the best as-deposited and VE-annealed devices under illuminated conditions. The device treated with vacuum annealing (VE-ann) exhibits a clear enhancement in performance across all key photovoltaic parameters compared to the as-deposited counterpart. This improvement correlates with the EQE results, attributing the gain to improved carrier collection efficiency and optimized bandgap grading due to Se-Te intermixing.

Specifically, the Short-Circuit Current Density (Jsc) increases significantly, rising from 25 mA/cm^2 to 28 mA/cm^2. The average efficiency parameters of Vac-ann and as-deposited samples are summarized in Table I.

Table I: Average efficiency parameters of VE-ann and As-deposited devices.

Device	FF [%]	Voc [%]	Jsc [mA/cm^2]	Eff [%]
VE-ann	67 ± 3	769 ± 14	27.9 ± 1	14.3 ± 0.3
As-dep	68 ± 2	748 ± 14	25.6 ± 1	13.0 ± 0.1

Furthermore, the Open-Circuit Voltage (Voc) and Fill Factor (FF) are also improved, indicated by the shift of the intercept to higher voltages and the squaring of the J-V curve, respectively. These enhancements confirm that the post-deposition vacuum annealing effectively passivates defects and optimizes the junction quality, reducing recombination losses.

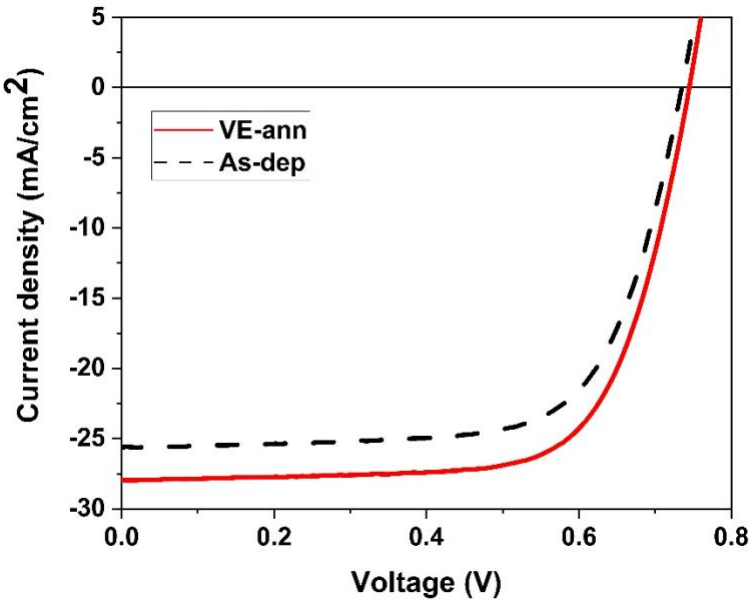

Figure 7.7: Current-Voltage characteristics of the best VE-ann and As-deposited samples.

7.6 Conclusion

CdSeTe/CdTe devices fabricated by evaporation, followed by vacuum annealing to mix CdSe and CdTe layers, show a marked improvement in average conversion efficiency compared to devices without annealing. Both XRD and Raman analyses confirm that the annealing step induces interdiffusion of Se and Te, while simultaneously reducing the amount of elemental Te present at the surface. Importantly, this annealing at 450 °C modifies the composition throughout the entire absorber layer. SIMS measurements reveal a higher Se-to-Te ratio near the junction in annealed (VE-ann) samples, consistent with a narrower band gap derived from EQE data. The XRD spectra also show a slight right shift in CdTe peaks for VE-ann devices compared to as-deposited (As-dep) samples, indicating increased Se incorporation into the bulk.

Optoelectronic characterization further highlights the benefits of annealing. VE-ann devices exhibit higher EQE across all wavelengths compared to As-dep devices, suggesting either reduced recombination centers or a thicker depletion region. The most significant difference lies in defect chemistry as-dep absorbers are dominated by the deep-level defect associated with Te

interstitials (negative-U centers), which are largely absent in VE-ann devices. Prior studies on CdS/CdTe cells have demonstrated that Te interstitials severely limit minority-carrier lifetime [10], and Cd-rich conditions are therefore beneficial. Our results indicate the same principle applies to CdSeTe/CdTe devices.

Thus, the observed performance gains in VE-ann devices can be attributed to a reduced presence of Te in the absorber. This finding also supports the broader conclusion that Se incorporation in CdTe-based devices improves minority-carrier lifetime [11,12] not only by bandgap engineering but also by altering stoichiometry specifically, by lowering the Te concentration.

Finally, VE-ann samples achieved a record efficiency of 14.7% for CdTe devices fabricated at low substrate temperatures with a reduced absorber thickness of only 2 µm, enabled by current densities exceeding 28 mA/cm².

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Chapter 8

Study of Absorber Thickness 0.5 µm – 0.8 µm

This work is published as:

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8.1 Introduction

The goal of this chapter is to determine the performance limits of the standard device structure when the absorber thickness is reduced to the ultra-thin range (0.5 µm – 0.8 µm). Driven by the need to comply with RoHS regulations and reduce material costs, this study investigates how reducing the thickness of the absorber impacts the depletion region width and carrier recombination. The objective is to identify the specific physical mechanisms that cause efficiency to drop when the absorber becomes too thin. Their cost-effectiveness and performance under various environmental conditions have positioned CdTe cells as a leading technology in the solar market. Recent innovations have focused on reducing material usage and environmental impact while enhancing electrical performance.

Moreover, despite CdTe being a stable compound and not releasing Cd (it is not on the list of carcinogenic materials) [1], it is subjected to RoHS (Restriction of Hazardous Substances) directives in the European Union. RoHS regulates the maximum concentration in consumer electronic items of elements considered dangerous to humans, and cadmium is limited to 0.01% or 100 ppm by weight. This means that using an absorber thickness below 0.8 µm would make CdTe-based devices on a 3 mm thick glass RoHS compliant, further expanding the possible applications of this technology [2].

One significant strategy for achieving these goals is the reduction of absorber thickness. A thinner absorber not only reduces material cost and consumption but also aligns with environmental regulations such as the Restriction of Hazardous Substances (RoHS) directive, which limits cadmium content in electronic devices. An absorber layer thinner than 0.8 µm on a 3 mm thick glass substrate complies with RoHS, opening the door for indoor applications and broader deployment.

This chapter presents a comprehensive study on ultra-thin CdSeTe/CdTe solar cells with varying absorber thicknesses, focusing on their electrical performance and material characteristics. The work investigates thickness-dependent efficiency and explores the mechanisms limiting ultra-thin device performance.

8.2 Device Fabrication

On Tec 12D- commercial glass substrate coated with FTO/TO (SnO_2: F/SnO_2) as previously described, we have deposited a bilayer of CdSe/CdTe with different thicknesses of CdSe/CdTe: 270/530 nm, 200/400 nm, and 200/300 nm, thus growing respectively a 0.8 µm, 0.6 µm and 0.5 µm thick absorber respectively.

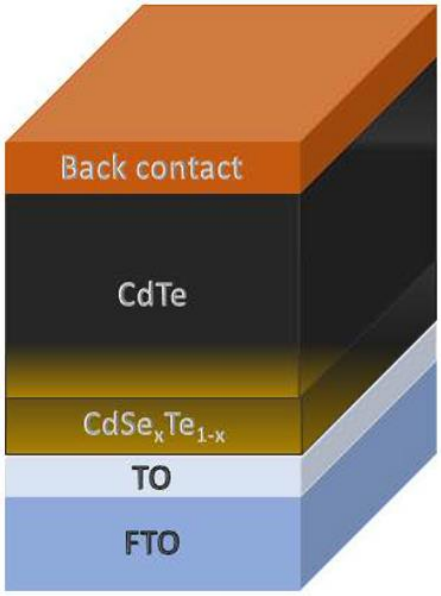

Figure 8.1: Sketch of devices configuration fabricated and analyzed.

In this case the $CdCl_2$ treatment also mixes the CdSe/CdTe layers to generate the expected $CdSe_xTe_{1-x}$ compound at the junction [3].

Finally, the samples are etched using a Br-MeOH solution, which clean the surface from the $CdCl_2$ residuals, simultaneously forming a Te-rich surface that promotes the synthesis of Cu_xTe at the CdTe/back contact junction [4]. Vacuum evaporation is used to deposit a 0.5 nm thick copper and a 30 nm thick gold layers to form the back contact (Fig.8.1).

8.3 Results and Discussion

The impact of the absorber thickness on the electrical properties of CdSeTe/CdTe devices is shown in Fig. 8.2. The performance parameters of these devices are presented in table 1. As expected, the best performances have been obtained with the thicker absorbers.

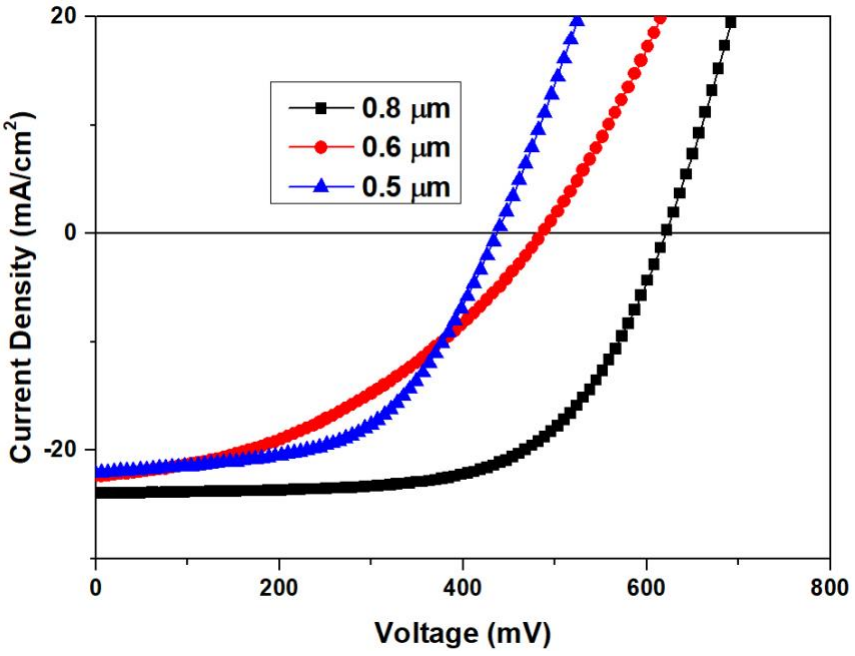

Figure 8.2: J-V curves of samples with a 0.5, 0.6 and 0.8 µm thick absorber.

With a 0.8 µm thick CdSeTe/CdTe the cells have reached an efficiency of 11%, with current densities of 25 mA/cm^2. By reducing the absorber thickness to 0.6 µm, current, Voc and FF decrease. With 0.5 µm mainly the Voc deteriorates, dropping to 440 mV in average.

EQE measurements explain the reduced current density for the thinner devices. As expected, the EQEs of the samples (see Figure 8.3) show a loss in response at long wavelengths when the absorber is thinned. Therefore, there is an absorption loss of those photons which are usually absorbed far from the junction.

TABLE 8.1: AVERAGE AND PEAK EFFICIENCY PARAMETERS OF THE DEVICES.

Thickness	FF (%)	Voc (mV)	Jsc (mA/cm^2)	Eff (%)
0.5 µm Best	57	447	22	5.8
Average	55.6±0.6	440±2	22.0±0.1	5.6±0.1
0.6 µm Best	56	601	21	7.3
Average	53.3±0.7	563±3	21.3±0.2	6.7± 0.2

0.8 µm Best	65	664	25	11
Average	66.3±0.6	661±1	25.0±0.1	10.9±0.2

The CV and DLCP measurements (Fig. 8.4) can estimate the net charge density (acceptor minus donor states) as a function of distance from the junction. Both shallow dopants and deep-level defects that can react to the AC signal are commonly included in standard C-V measurements. On the other hand, DLCP depends on the junction capacitance's non-linear relationship with the AC driving amplitude. By using this non-linearity, DLCP preferentially examines the free carrier density at the depletion edge, making it relatively insensitive to deep bulk defects.

Therefore, the difference between CV (open dots) and DLCP curves measured in the same condition indicates the number of deep states. While with a 0.8 µm thick absorber, CV and DLCP profiles overlap, with a 0.5 µm thick absorber the higher net charge density measured by DLCP compared to CV suggests the presence of deep donor defects.

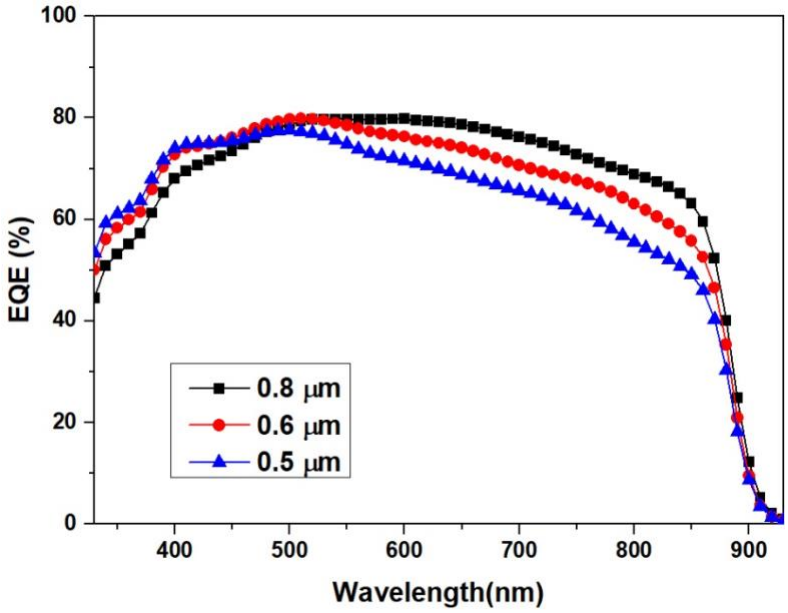

Figure 8.3: Comparison of external quantum efficiency measurement of samples with a 0.5, 0.6 and 0.8 µm thick absorber

Moreover, for the 0.5 µm thick absorber, the profiles suddenly rise between 0.2 µm and 0.3 µm from the junction; this is normally attributed to the influence of the back contact, suggesting that the absorber is completely depleted. This favors the carriers' recombination near the back contact, impacting on the reduction of all the efficiency parameters.

Another important observation is that the net charge density around $6*10^{15}$ cm^{-3} for the 0.5 µm thick absorber sample, is higher than the $1*10^{15}$ cm^{-3} for the 0.8 µm absorber thick device, leading to a narrower depletion region width. Moreover, both the net charge densities are much higher than the one (10^{14} cm^{-3}) of the 2 µm thick absorber devices [5]. To analyze if this is due to the CdSe/CdTe ratio or to the reduced thickness of the devices, considering also the (higher) copper concentration for thinner absorbers, CV/ DLCP analysis has been performed on additional samples. Fig. 8.5 presents CV/ DLCP measurements on 0.8 µm thick devices with a reduced CdSe/CdTe ratio (150 nm CdSe /650 nm CdTe) compared to the previous sample.

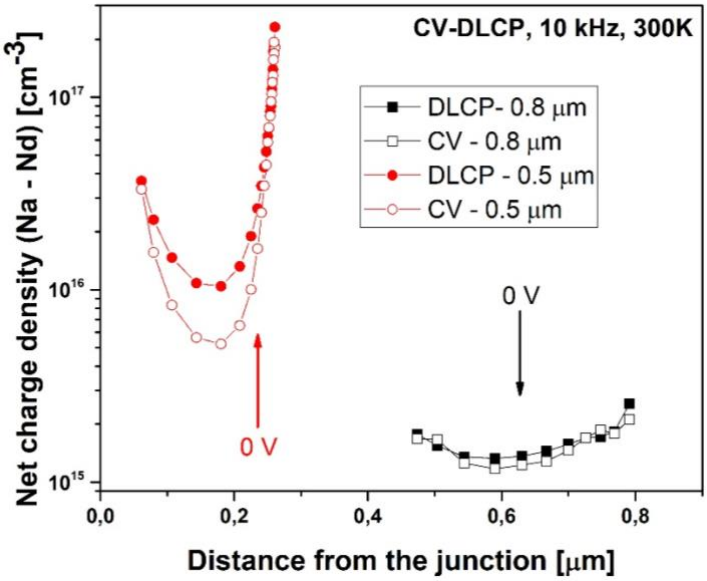

Figure 8.4: CV (open dots) and DLCP (full dots) of samples with a 0.5 and 0.8 µm thick absorber.

In figure 8.5, the red profiles refer to a sample containing the standard 0.5 nm thick copper layer, while the blacks belong to a copper-free device. Despite the different CdSe/CdTe ratio, the sample containing copper shows the same net charge density and a similar depletion region width compared to the 0.8 µm thick device.

By avoiding the intentional introduction of copper, the net charge density reduces, causing the complete depletion of the absorber layer as shown in CV/DLCP profile; in fact, the black profiles suddenly rise towards the back contact, revealing its influence. Figure 8.6 shows the current-voltage characteristics of 0.8 µm thick samples, with and without intentional copper doping, demonstrating the negative impact of complete depletion of the absorber. In fact, the red curve (Cu-doped device) exhibits higher FF and Voc compared to the black one (no Cu), suggesting lower recombination.

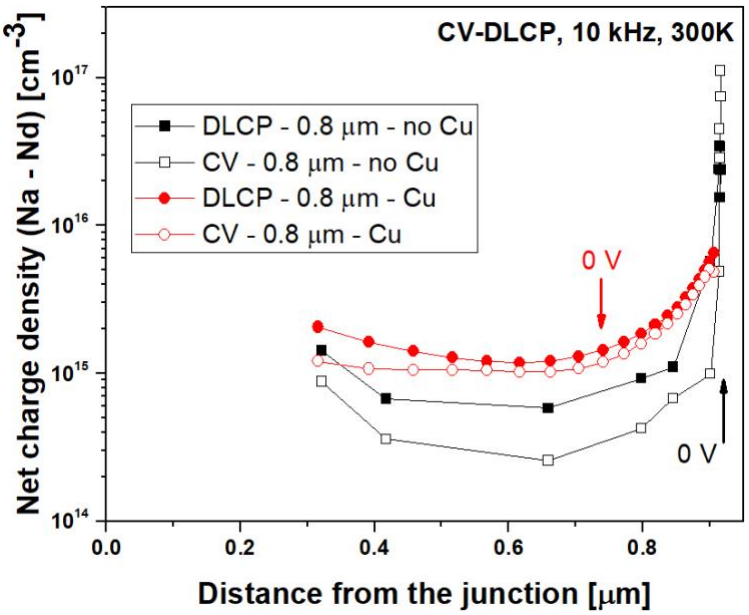

Figure 8.5: CV (open dots) and DLCP (full dots) measurements on 0.8 µm thick samples with (red lines) and without (black lines) copper.

On the other hand, the net charge density of the copper-free device still results higher than that of our 2 µm thick samples.

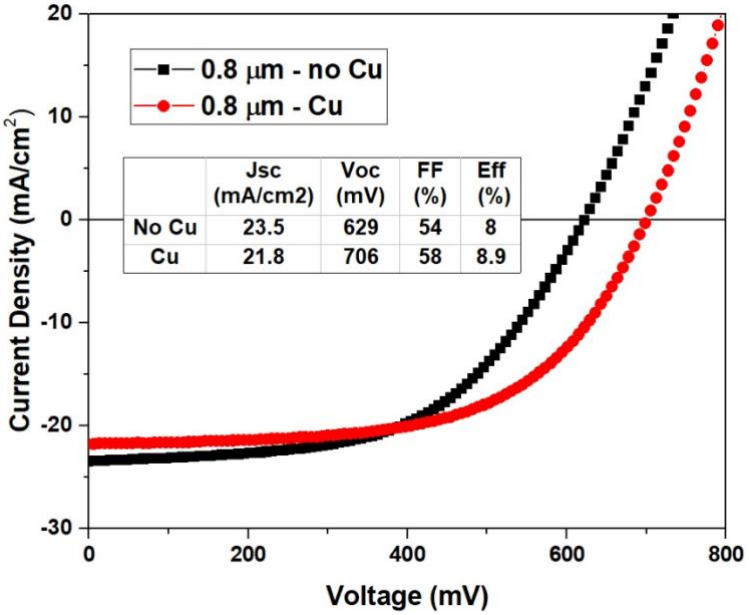

Figure 8.6: JV curves of 0.8 µm thick samples with (red lines) and without (black lines) copper doping.

8.4 Conclusion

CdSeTe/CdTe devices with reduced absorber thickness between 0.5 µm and 0.8 µm have been fabricated and studied. An ultra-thin absorber can reduce the material impact in terms of availability, cost, and environmental effects. Currently, in our laboratory, samples with a 0.8 µm thick absorber (which satisfies RoHS rules for consumer electronics) have reached efficiencies of 11 %, with good current densities of 25 mA/cm^2 and decent Voc and FF values. By further reducing the absorber thickness, all the efficiency parameters decrease. As expected, EQE shows the loss of carriers at long wavelengths for the thinner absorbers, explaining the lower current. On the other hand, CV-DLCP profiles indicate a higher presence of deep defects for the thinner absorbers. Moreover, these measurements suggest that in the 0.5 µm case, the absorber is completely depleted, favoring the recombination of the carriers near the back contact. This points out that to further reduce the thickness of the absorber, an electron reflector should be introduced.

On the other hand, thinner absorbers reveal higher net charge densities compared to our 2 µm thick devices, implying a reduction of the depletion region width. For 0.8 µm thick devices, the absorber is completely depleted for un-doped samples but not for Cu-doped ones, revealing the importance of Cu introduction. This suggests that it is worth exploring other doping techniques, such as $CuCl_2$ [6], to balance the correct doping concentration for such thin absorber thicknesses.

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Chapter 9

Effect of Selenium on the Physical and Electrical Properties of Ultra-Thin CdSeTe/CdTe Solar Cells

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9.1 Introduction

Based on the experimental results of the previous chapter, the 0.8 µm absorber thickness was identified as the optimal candidate for ultra-thin applications, as it successfully balances material reduction with electrical functionality. Having selected this specific thickness as the viable platform for RoHS-compliant devices, it is now essential to understand how the material composition affects its performance.

The primary goal of this chapter is to investigate the effect of selenium concentration on the physical and electrical properties of the 0.8 µm absorber. While selenium is known to enhance performance in standard thick devices, its diffusion kinetics and impact on grain growth within a constrained 0.8 µm layer are not yet fully understood. By fixing the absorber thickness at 0.8 µm and systematically varying the CdSe/CdTe ratios, this study aims to determine the ideal Selenium profile that maximizes the efficiency and stability of this selected ultra-thin configuration.

Over the past twenty years, several key improvements have resulted in advancements in CdTe photovoltaic (PV) efficiency, which has reached 23.1 % [1]. One significant enhancement is related to selenium introduction to form a graded $CdSe_xTe_{1-x}$/CdTe absorber. The presence of $CdSe_xTe_{1-x}$ near the junction reduces the band gap to around 1.4 eV, broadening the wavelength range for photocurrent generation [2]. This approach, coupled with eliminating the CdS window layer and its parasitic absorption, significantly increases the short-circuit current density (Jsc), which now exceeds 30 mA cm^{-2} [3].

Studying the impact of selenium and its concentration in an ultra-thin absorber layer becomes a very important issue. In order to understand the mechanisms of Se impact on ultra-thin devices, we have fabricated and analysed devices with different CdSe/CdTe ratios keeping the overall absorber thickness at 800 nm.

9.2 Device Fabrication

For this specific study, we have reduced the thickness of the absorber from our standard 2 µm [10] to 0.8 µm. Precisely, we have fabricated different devices depositing CdSe/CdTe with various ratios: 75/725 nm, 150/650 nm, 270/530 nm, and 400/400 nm. During the deposition, the film thickness is measured using the quartz crystal microbalance placed next to the substrate holder and cross-checked with a stylus profilometer.

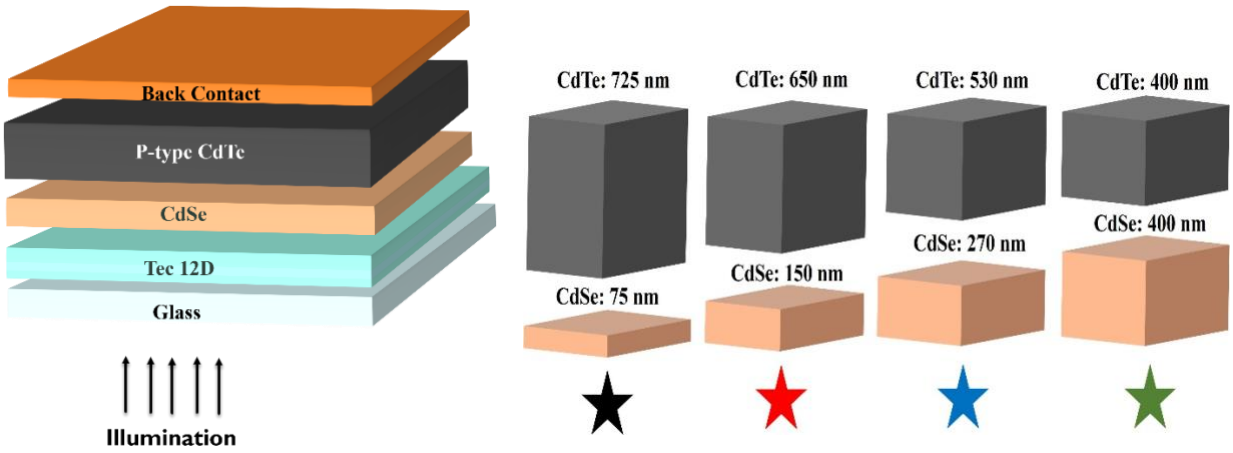

Figure 9.1: Sketch of the configuration of the devices fabricated and analyzed (the colored star indicates the colors that will be used in the following graphs for identifying the different cases).

9.3 Characterization methods

External Quantum Efficiency (EQE) measurements were recorded using a monochromator (Lot-Oriel Omni-λ300) and a halogen lamp (100 W) as the incident light in AC mode. The monochromatic light was mechanically chopped at a frequency of 75 Hz, and the photocurrent response was measured using a lock-in amplifier. The system was calibrated with Thorlabs S120VC and S122C photodiodes. The thickness of the film is cross-checked with a customized profilometer.
Electron backscatter diffraction (EBSD) analysis was performed with a Helios G4 (Thermo Fisher Inc) equipped with a Xenon-Plasma Focused Ion Beam (pFIB) and a CMOS detector, using an electron beam accelerating voltage of 5kV and a current of 6.4 nA.

Cathodoluminescence (CL) measurements were performed at room temperature in a thermal field emission SEM equipped with a Monarc Pro CL system, with an electron beam accelerating

voltage of 5kV and a beam current of 1.6 nA. The CL maps were acquired using a 200 µs dwell time per pixel.

9.4 Results and discussion

9.4.1 Structural and electrical analysis

X-ray diffraction (XRD) analysis has been conducted to investigate the crystallographic structure of the absorber and understand how the incorporation of selenium affects its composition. Fig 9.2(A) shows the XRD patterns of treated absorbers fabricated with different CdSe/CdTe ratios. Key peaks are identified: the dominant orientation of the CdTe is (111), with smaller peaks at (220), (311), (400) and (331). Moreover, smaller peaks attributed to CdSe are detected, suggesting the presence of remains of this compound. On the right, Fig. 9.2(B) displays a close-up of the dominant CdTe peaks, highlighting that as the CdSe thickness increases, these peaks shift to the higher theta (right side). This peak shift indicates enhanced selenium diffusion and its subsequent incorporation into the crystal lattice deeper within the bulk [11].

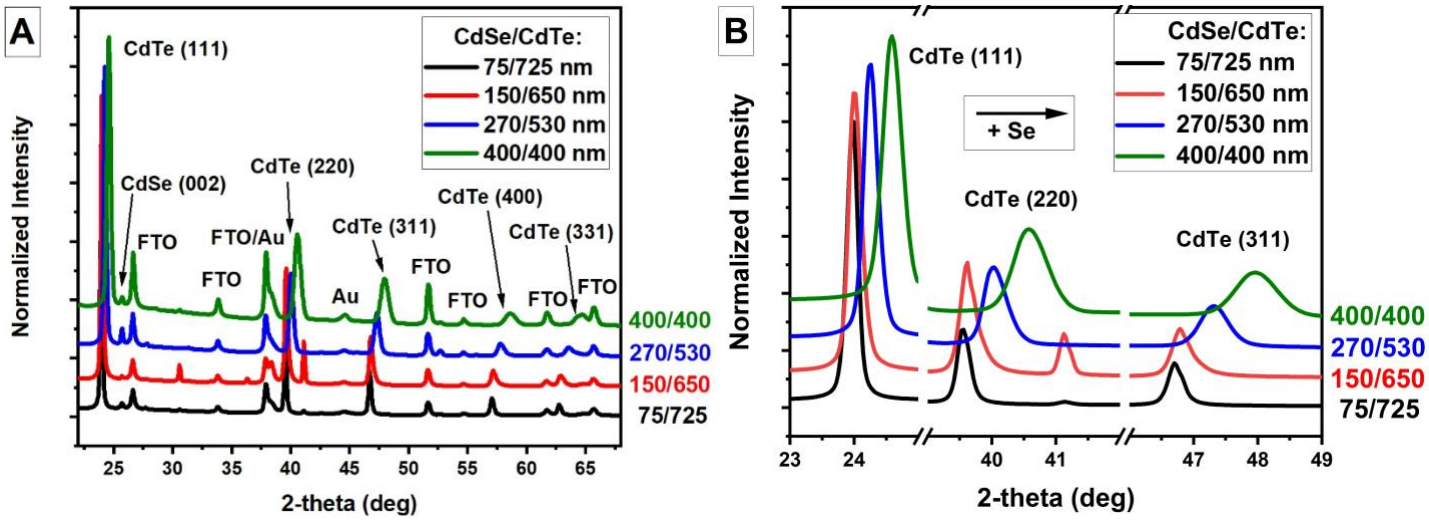

Figure 9.2: XRD analysis of samples fabricated with different CdSe/CdTe ratios: (A) 22-68 deg range spectra; (B) close-up of the main CdTe peaks.

Furthermore, the peaks become broader by increasing the thickness of the CdSe layer. According to the kinematic scattering theory, the broadening of the peaks can be attributed to increased lattice defects or a reduction in the crystallite size to less than one micron [12]. For thicker CdSeTe/CdTe absorbers, it has already been experimentally observed that the introduction of selenium into the absorber leads to the formation of a CdSeTe layer with smaller grains towards the junction and a second layer of larger grains from the bulk to the back contact (the absorber

tends to form a bi-layer: CdSeTe at the front and CdTe at the back) [13], [14]. This effect could also be expected for ultrathin absorbers; the broadening of the peaks could then suggest a preponderance of small grains as the CdSe thickness increases, due to a higher Se incorporation in the CdSeTe compound. Especially in the case of 150/650, we can observe some minor peaks around 2-theta at 31, 41 and 52 degrees, these can be easily attributable to $CdTeO_x$, occurring with $CdCl_2$ activation treatment [15].

Fig. 9.3 presents AFM images of $CdSe_xTe_{1-x}$/CdTe films formed by activating a 75/725 nm (Fig. 9.3(A)) and a 400/400 nm (Fig. 9.3(B)) CdSe/CdTe bi-layer. The morphology of the absorber is very different, the grains of the 400/400 nm CdSe/CdTe sample are visibly smaller compared to the 75/725 nm, which has much more compact grains. This confirms the hypothesis that the broadening of the XRD peaks is due to a reduction of the absorber layer's grain size by increasing the CdSe layer thickness.

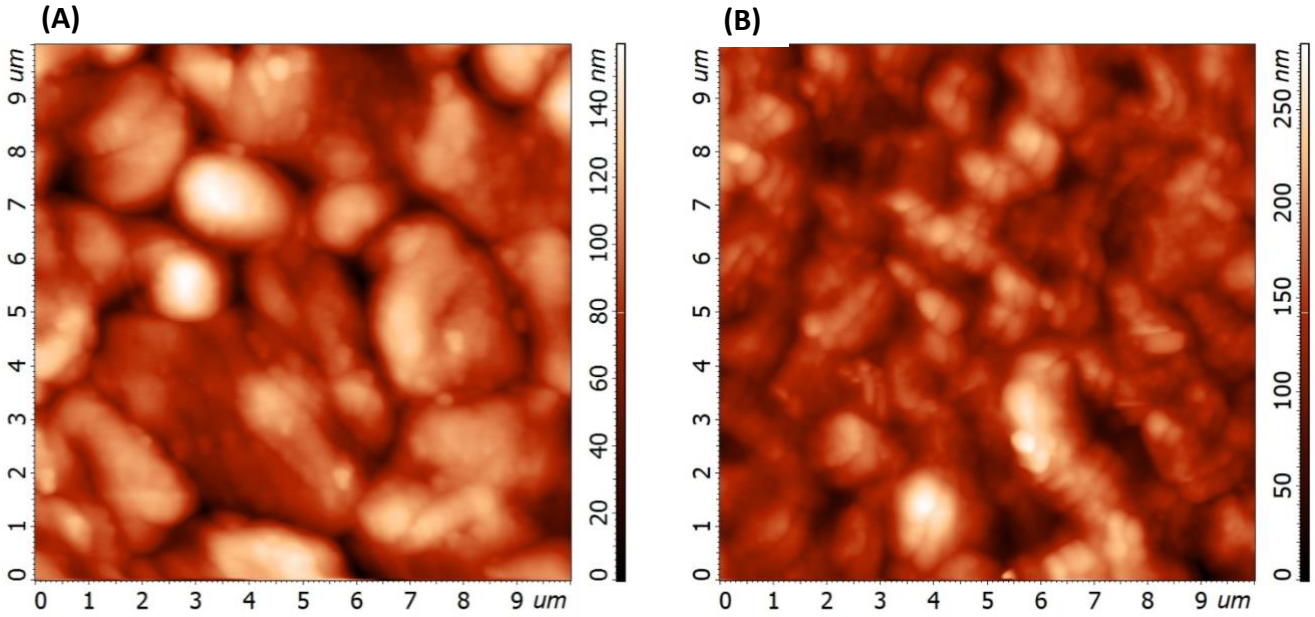

Figure 9.3: AFM images of absorber surface of (A) 75/725 nm (B) and 400/400 nm CdSe/CdTe samples.

SIMS analysis has been carried out on the samples to address the selenium distribution into the absorbers after the $CdCl_2$ treatment. With a 75 and 150 nm thick CdSe layer, the Se profiles decrease towards the back contact, suggesting a graded band gap absorber (see Fig. 9.4). Conversely, the corresponding Te profiles are nearly flat. Still, it must be considered that the yield of SIMS measurements depends on the element. As expected, in the 400/400 nm case, the measurement shows a higher amount of Se than the other samples and detects a lower amount of Te. In this case, the Se profile is almost flat, showing only a slight decrease in counts per second

towards the back contact, suggesting the formation of a nearly homogeneous CdSeTe composition along the entire depth of the absorber layer. However, in all the devices, Se diffuses throughout the layer. Comparing the devices at corresponding sputtering depths, as the initial CdSe thickness increases, the samples show a more selenium-rich compound throughout the absorber. As already mentioned in the previous paragraph, the presence of Se leads to smaller grains than those of CdTe. Thus, the increasing presence of selenium in the bulk and towards the back contact explains the smaller grains on the back surface of the absorber observed with AFM and the broadening of the XRD peaks in the samples fabricated with thicker CdSe layers.

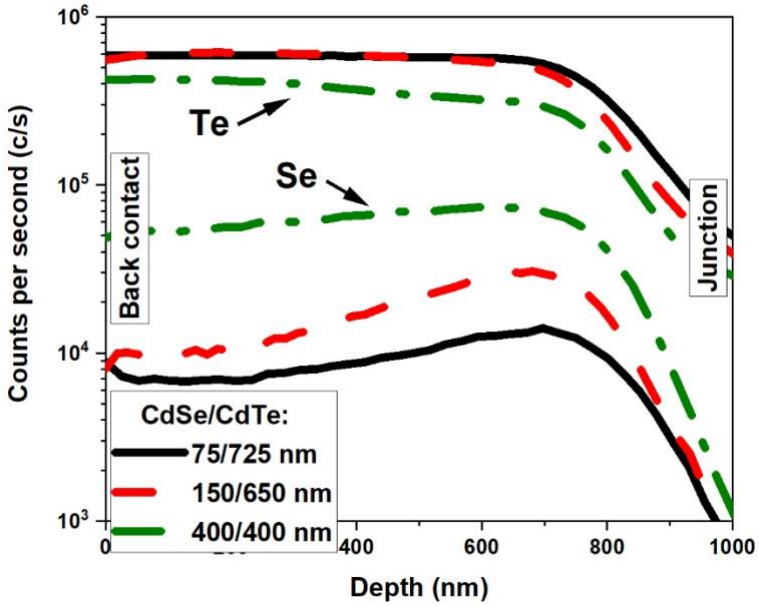

Figure 9.4: SIMS depth profiles showing Se and Te distribution in absorbers fabricated with different CdSe/CdTe ratios.

The samples were subjected to EQE analysis (see Fig. 9.5) to verify whether selenium, besides being distributed throughout the absorber, reduces the band gap near the junction compared to pure CdTe, increasing the absorption at long wavelengths. Despite the small CdSe peaks detected by XRD, the EQE spectra do not reveal a parasitic absorption below 700 nm for the residual CdSe layer [16], suggesting a quasi-complete intermixing of CdSe and CdTe in all the samples. This appears to be an advantage of using a thin absorber since it was shown that parasitic absorption due to incomplete mixing occurs if 200-400 nm of CdSe is evaporated for a total absorber thickness of 3.5 µm [17].

As the thickness of the CdSe layer in the devices is increased from 75 to 270 nm, the spectra show a right shift of the response at long wavelengths, confirming the narrowing of the band gap of the absorber. Taking the value corresponding to the maximum negative derivative of the EQE curve

at long wavelengths [18], the bang gaps are estimated to be 1.44 eV with a 75 nm thick CdSe and 1.39 eV with a 270 and 400 nm thick CdSe. A 270 nm thick CdSe on a total absorber thickness of 800 nm is sufficient to reach the minimum band gap achievable with a $CdSe_xTe_{1-x}$ compound. Moreover, the 400/400 sample denotes a noticeable decrease in EQE response at all wavelengths; this loss is not localized but appears uniform throughout the absorber. Such a reduction in EQE generally suggests a higher concentration of defects causing recombination in the entire absorber. In this specific case, one could hypothesize that a more selenium-rich CdSeTe could be associated with a reduced photoactivity; on the other hand, another probably more suitable explanation is that the reduction of the grain size due to the increasing of Se concentration in the bulk (as highlighted by the measurements discussed previously) implies a higher amount of grain boundaries and so a significant carrier recombination.

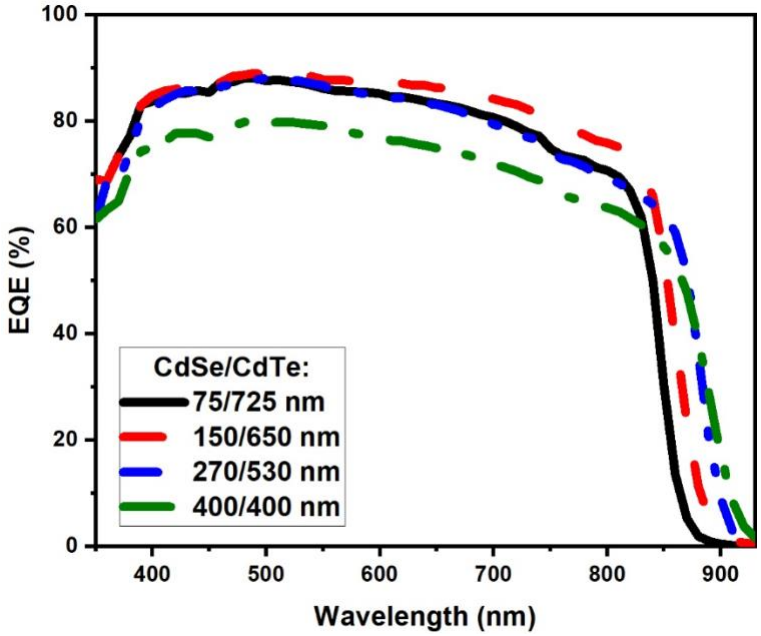

Figure 9.5: Comparison of EQE of samples fabricated with different CdSe/CdTe ratios.

To investigate whether this decrease in EQE response is related to the grain size in the absorber and, hence, the amount of grain boundaries, EBSD analysis was performed at Loughborough University in collaboration with Prof. Michael Walls on the cross-section of 400/400 nm and 75/725 nm samples. EBSD images provide a microstructural analysis, where the colored regions represent the crystallographic orientations of individual grains. For the device with lower selenium concentration (see Fig. 9.6A), the grains are approximately equiaxed, with an average size of 1.1 µm throughout the absorber layer. Moreover, most grains occupy the entire thickness of the absorber, from the front to the back surface. On the other hand, the 400/400 nm sample exhibits a smaller grain size of 0.86 µm on average (see Fig.9.6B). A few grains extend from the front to the back surface, but mostly, the structure is disordered with smaller overlapping grains; dark areas highlight the presence of voids. Interestingly, no sample shows evidence of a CdSeTe/CdTe bilayer structure, as observed for thicker absorbers [13]. This analysis confirms that with the increase of the CdSe thickness, the grain size reduces in the whole absorber, not only near the junction; and this is because by using a 0.8 µm thick absorber, there is no formation of a CdSeTe/CdTe bi-layer structure. Moreover, it suggests that a high selenium concentration leads to a disordered arrangement of the grains, and also to the formation of voids (confirmed by cross-sectional backscatter SEM images, not shown here), contributing to the reduced EQE response

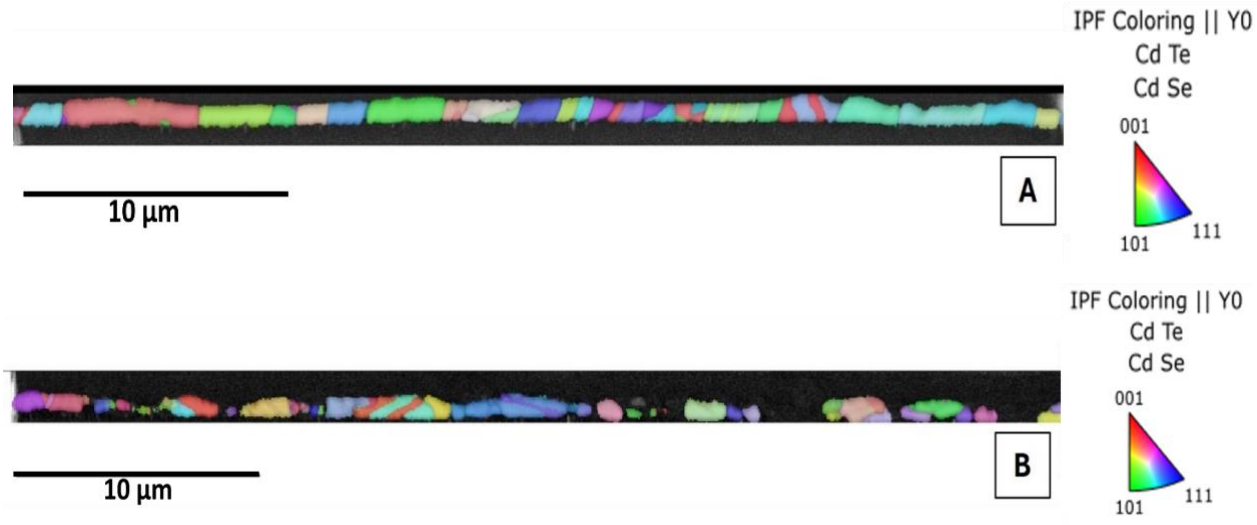

Figure 9.6: EBSD analysis of samples (A) 75/725 nm and (B) 400/400 nm in cross-section.

seen before.

SIMS analysis indicates a different Se diffusion and EQE analysis points out the presence of a different band gap in the 75/725 and 150/650 nm absorbers; however, the absence of a CdSeTe/CdTe bi-layer structure highlighted by EBSD images is unusual. To investigate this phenomenon in detail, also at Loughborough University, SEM was used to collect the CL hyperspectral map of the 75/725 and 400/400 nm samples compared to the standard thick

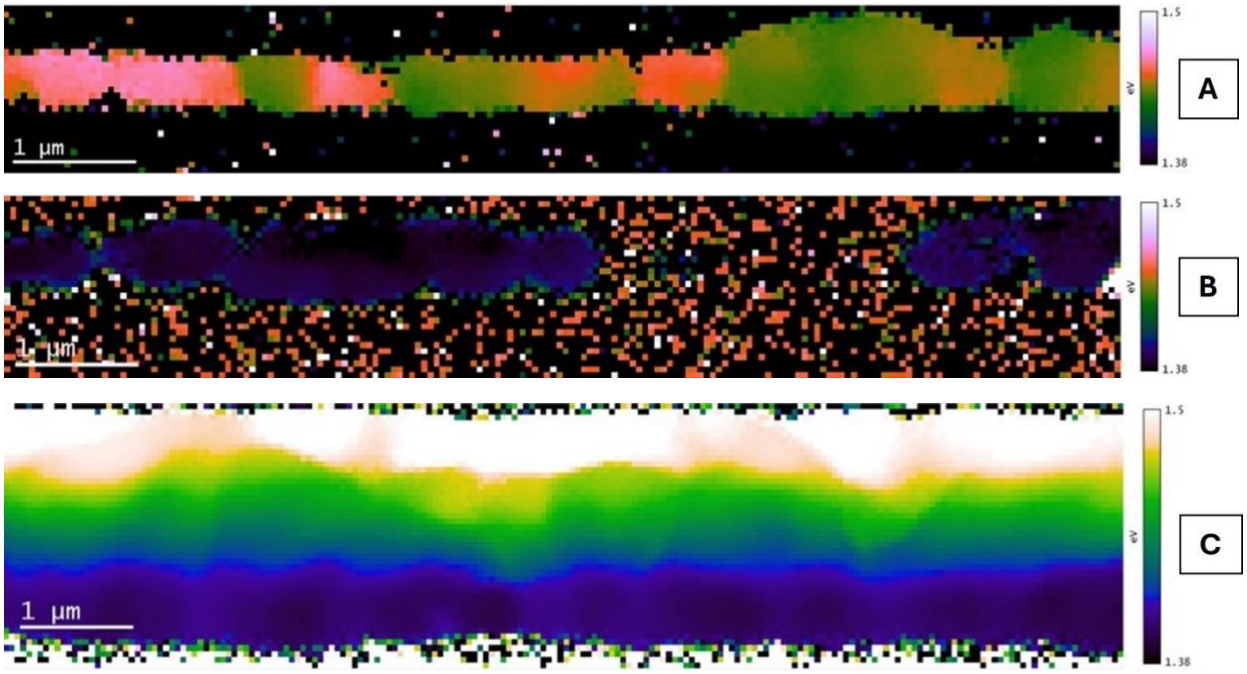

Figure 9.7: Hyperspectral CL map (eV) of the (A) 75/725 nm, (B) 400/400 nm, and (C) 300/2000 nm devices

absorber sample in cross-section (see Fig 9.7); colour variations correspond to emission energy (eV) differences, showing localized variations in the band gap. Fig. 9.7(B) confirms the formation of a nearly homogeneous CdSeTe composition of the absorber layer for the 400/400 nm case, as assumed by SIMS profiles. The dark blue region in the absorber in Fig. 8.7(B) corresponds to a uniform bandgap energy of 1.39 eV. Note that the scattered red and white pixels surrounding this region of the absorber are due to detector noise. On the other hand, for the 75/725 nm case (Fig. 9.7(A)), the CL signal shows a band gap ranging from 1.43 eV to 1.47 eV. However, the map suggests that the band gap is not graded from the front junction to the back, perpendicularly to the substrate, but varies from grain to grain. Selenium is supposed to diffuse along the grain boundaries and subsequently into the CdTe grains through the grain boundaries [19]. Figure 9.7c shows that with a standard thickness, the absorber shows its expected grading, highlighting that the behavior described above is to be addressed to the ultra-thin absorber.

However, the question of whether, during recrystallization, Se preferentially diffuses in some grains rather than others has never been addressed. One hypothesis is that this might depend on the initial orientation of the grains: from the grain boundaries, the selenium enters the near grains with an orientation more favorable to its diffusion.

With a CdTe thickness of less than 800 nm, the size of the grains extends from front to back contact even for as-deposited samples, i.e. before the activation treatment; selenium, therefore, appears to be unable to penetrate some grains whose orientation is possibly unfavorable to its diffusion. In the case of a 2 to 3 µm thick CdTe, the thickness of the as-deposited absorber is composed of a few layers of grains; selenium diffusing across grain boundaries can then surround the grains of the first layer/layers, finding the most energetically favorable path to diffuse inside as well. This also explains why, using larger thicknesses, a CdSeTe/CdTe bi-layer is formed. The diffusion of Se in the first layers of grains forms the CdSeTe layer, while Se does not affect the subsequent grain layers, which, therefore, remain CdTe. This bi-layer cannot form if the grains of the as-deposited CdTe extend throughout the entire thickness of the film.

The integration of EBSD, CL and EBSD GB misorientation measurement (Aztec) can identify if this supposition is correct. In Figure 9.8, the specific area of the 75/725 nm case, depicted in Figure 9.7(A), is analyzed by Aztec: grain boundary (GB) misorientation angles can be determined for any grain. In this case we have isolated two boundaries; the LHS boundary (GB1) has a misorientation angle of 15.14º, a low angled boundary whose neighboring grain interior's coloring in the hyperspectral CL map indicates that the GB acts as a barrier between a relatively high Se content grain to its left, and low Se content to its right.

The RHS GB misorientation angle of 59.93º (GB2) is much higher and is classified as a Σ3 boundary. The higher grain boundary misorientation angle has allowed more lateral Se diffusion, leading to lower band gap readings at neighboring grain interiors, as shown in the CL hyperspectral map. Essentially, higher grain boundary misorientation angles encourage more Se diffusion between grains, whereas lower grain boundary misorientation angles inhibit Se diffusion.

To further investigate the impact of selenium concentration on the presence of defects, CV and DLCP analyses were performed on the samples (see Fig. 9.9). CV and DLCP measurements enable the estimation of the net charge density (difference between acceptor and donor states) as a function of distance from the junction. Since deep defects have minimal impact on the DLCP profiles (solid dots), the discrepancy between the CV (open dots) and DLCP curves, recorded under identical frequency and temperature conditions, reveals the number of deep defects [20]. Furthermore, the arrows correspond to the point of the measurement taken when the DC bias voltage is equal to 0, estimating the width of the depletion region. As the CdSe thickness increases, CV profiles go from being lower to being higher than DLCP profiles, suggesting a different nature of the deep defects. For lower selenium concentrations, the deep defects compensate the net charge density, suggesting their donor nature.

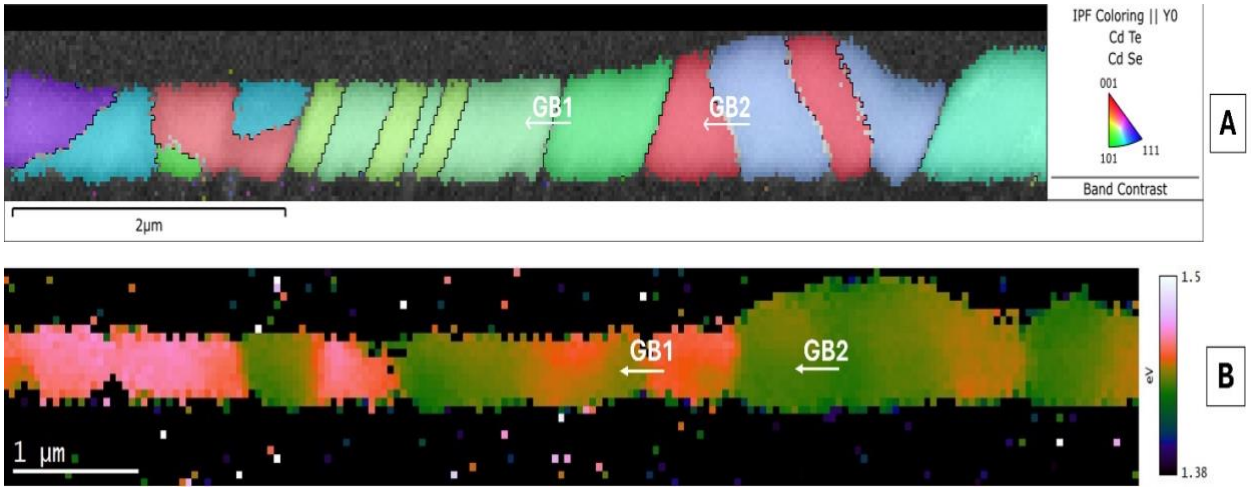

Figure 9.8: (A) EBSD map and (B) cathodoluminescence (CL) map of the same region of the CdTe absorber, showing two grain boundaries labelled GB1 and GB2. These boundaries are marked to enable direct comparison between crystallographic features and CL response. The misorientation angles are 15.14° for GB1 and 59.93° for GB2, respectively.

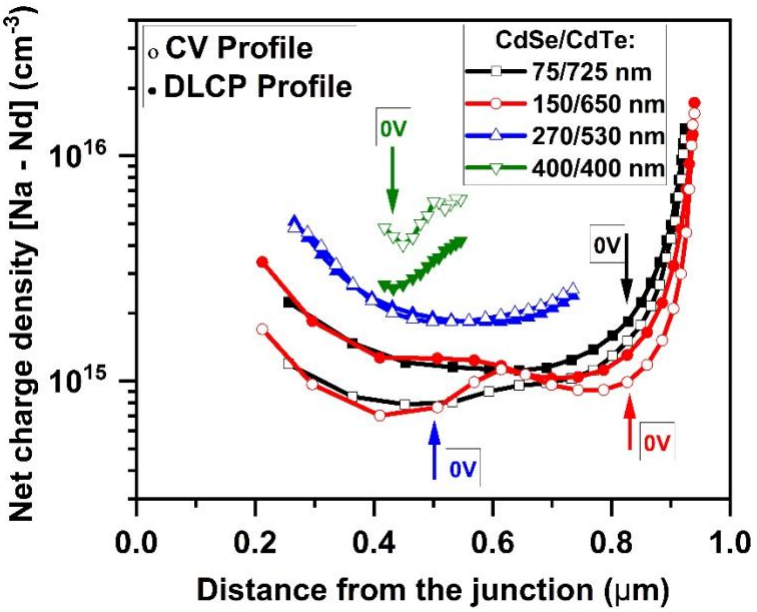

Figure 9.9: Comparison between CV (open dots) and DLCP (full dots) profiles of samples fabricated with different CdSe/CdTe ratios.

Furthermore, the profiles reveal a clear trend: as the selenium content grows, the net charge density increases, leading to a narrower depletion region width. This observation is particularly significant given the thin nature of the layers since there is a risk of having a fully depleted absorber, which implies recombination at the back surface, limiting the voltage [21]. The sudden rise of the profiles towards the back contact for the thinner CdSe cases is a measurement artefact, indicating that the absorber is completely depleted [22], as also suggested by the arrows, which are located at a distance greater than 0.8 µm from the junction. 270 nm is an optimal CdSe thickness to achieve sufficient net charge density (approximately $2*10^5$ cm^{-3}) to reduce the depletion region width to around 500 nm; moreover, in this case, CV and DLCP profiles overlap, suggesting a reduced number of deep defects. In contrast, the sample fabricated using a 400 nm thick CdSe layer shows the highest concentration of deep defects, possibly due to the disordered arrangement of the grains and the voids seen with EBSD analysis.

9.4.2 Performance of the devices

But how does the impact of the selenium concentration on the absorber structure influence the performance of the devices? Table I presents the peak and average efficiency parameters of samples fabricated with different CdSe/CdTe ratios, while Fig. 8.10 shows the current-voltage characteristics of the best cells. By increasing the thickness of the CdSe layer from 75 to 270 nm, the average Voc slightly decreases, possibly due to the narrowing of the band gap at the junction; however, this leads to a mild rise of the Jsc.

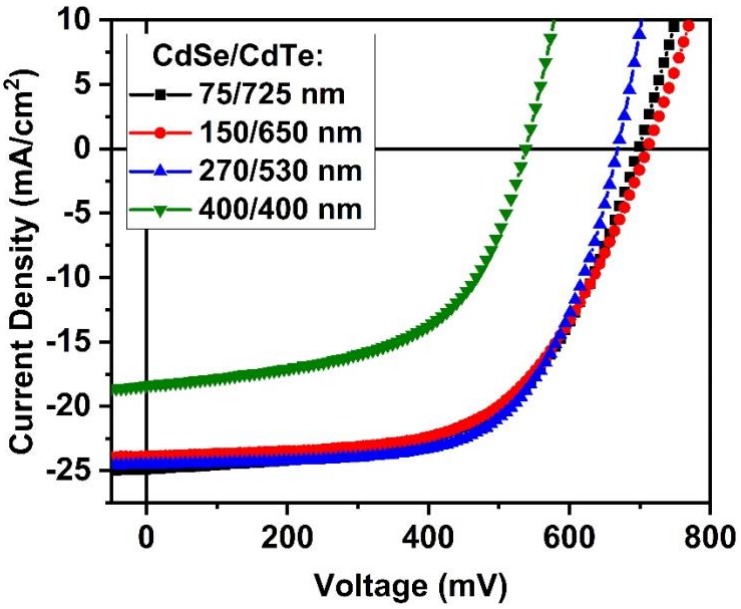

Figure 9.10: JV-curves of the samples fabricated with different CdSe/CdTe ratios.

On the other hand, the FF has a more substantial improvement from 58 to 62 % on average. This could indicate a reduced recombination in the depletion region [23] and thus be related to the increased selenium concentration since Se passivates grain boundaries and enhances carrier lifetime [14]. Overall, the efficiency of the cells increases modestly from 9.7 to 10 % on average. The slight difference in cell performance can also be observed by comparing the JVs of the peak cells in Fig. 9.10.

By further increasing the thickness of CdSe to 400 nm, the performance of the devices drops to 5 % on average, due to the lowering of all the efficiency parameters; which is not surprising, given the previous analysis. The lower Jsc value, compared to the other samples, was already evident from the EQE measurements, which we related to the smaller size of the grains and their disordered arrangement due to the higher selenium concentration. However, the consequent enhanced carrier recombination also explains the Voc and FF drop.

Previous studies have demonstrated that Br-MeOH processes, being Cd-selective etchings, also convert regions of grain boundaries from CdTe to elemental Te, reducing their band gap to 0.33 eV.

Table 9.I: peak and average efficiency parameters of samples fabricated with different CdSe/CdTe ratios.

Sample: CdSe/CdTe		FF(%)	Voc (mV)	Jsc (mA/cm^2)	Eff (%)
75/725	Best	58	699	24.9	10.1
	Avg	58 ± 1	699 ± 1	23.8 ± 2	9.7 ± 0.6
150/650	Best	59	713	23.9	10.1
	Avg	58 ± 1	685 ± 37	24.1 ± 0.9	9.6 ± 0.4
270/530	Best	64	671	24.5	10.5
	Avg	62 ± 2	673 ± 4	24.3 ± 0.6	10.0 ± 0.4
400/400	Best	55	545	18.3	5.5
	Avg	52 ± 5	484 ± 82	20.0 ± 2	5.0 ± 0.7

This can be seen as an extension of the back contact that diffuses into the bulk. Therefore, in the case of ultra-thin absorbers, the increased recombination due to elemental tellurium in the grain boundaries would lead to Voc losses [24].

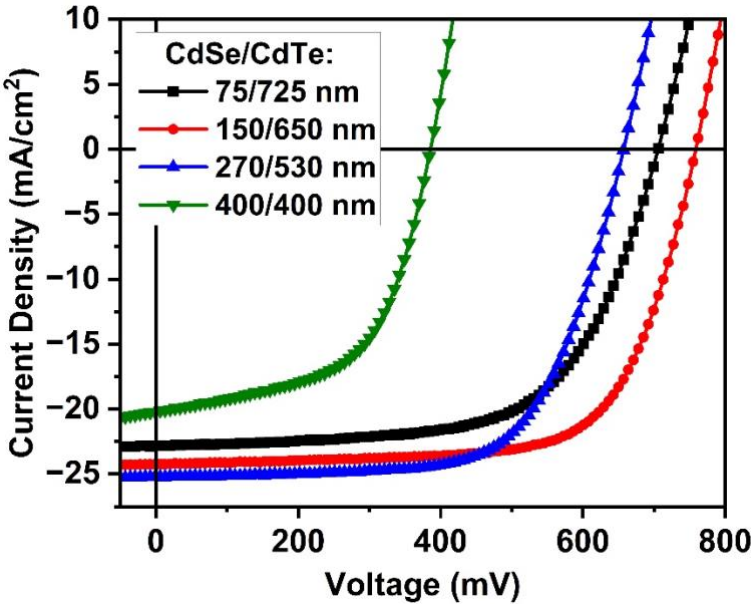

Figure 9.11: JV curves of the samples fabricated with different CdSe/CdTe ratios without Br-MeOH etching.

For this reason, instead of using the Br-MeOH etching, recently, the back surface of the absorbers was washed with distilled water after the activation treatment. Avoiding the etching step allowed

us to achieve higher-efficiency devices, whose JV curves are presented in Fig. 9.11 and the related efficiency parameters in Table II. This optimization has strongly improved the average FF of all the samples and the Voc of the devices with the lowest Se concentration. Without elemental Te, the active layer is wider, reducing the risk of a fully depleted absorber. This is particularly effective for cells where the net charge density is reduced by low Se concentration.

Table 9.II: peak and average efficiency parameters of samples fabricated with different CdSe/CdTe ratios without Br-MeOH etching.

Sample: CdSe/CdTe		FF (%)	Voc (mV)	Jsc (mA/cm^2)	Eff (%)
75/725	Best	63	706	22.8	10.2
	Avg	61 ± 2	685 ± 25	23.1 ± 0.4	9.8 ± 0.5
150/650	Best	69	762	24.3	12.8
	Avg	67 ± 2	753 ± 11	24.6 ± 0.6	12.4 ± 0.4
270/530	Best	65	664	25.3	10.9
	Avg	64 ± 1	659 ± 4	25.4 ± 0.2	10.8 ± 0.2
400/400	Best	56	391	20.1	4.4
	Avg	56 ± 2	384 ± 7	20.1 ± 1	4.3 ± 0.1

Without the Br-methanol step, the 150/650 case is the best trade-off between the reduced band gap value at the junction and the increased net charge density, due to the insertion of selenium, reaching an average Voc of 753 mV. These cells have achieved peak efficiencies close to 13 %, which is noticeable considering the thin absorber (800 nm). Again, fabricating devices with a 1 to 1 CdSe/CdTe ratio results in a drop in all efficiency parameters.

9.4.3 Stability of the samples

The samples have been subjected to accelerated stability tests (AST), to investigate how the selenium concentration could affect the stability of the devices. Precisely, 10 cells for each type were kept at 80 °C under one sun illumination in an open circuit condition, and their efficiency parameters were periodically measured after cooling down; the average efficiency, FF, Jsc and Voc normalized to their initial values versus time are presented in Fig. 9.12. In this case, all the devices

were subjected to the above-mentioned etching treatment. All samples show a stable current density over time, in line with what we have already reported for devices with a 7 µm thick CdTe absorber [25]; only the cells with the highest Se concentration show a slightly unstable Jsc. Except for the devices with an initial CdSe thickness of 75 nm, these thinner, selenium-containing samples demonstrate a more substantial Voc reduction than the thicker CdTe; in contrast, the FF is stable or even improved over time. Overall, samples with intermediate selenium concentrations show stability consistent with our CdS/CdTe devices; samples containing less selenium are more stable, while those fabricated with a CdSe/CdTe 1 to 1 ratio are more unstable. Thus, the degradation over time of the cells depends on the initial CdSe/CdTe ratio; by increasing Se concentration, the stability of the devices reduces. Se insertion strongly affects the degradation of the Voc. In CdS/CdTe cells, Voc degradation was attributed to Cu diffusion from the back contact; Cu is a fast diffuser that accumulates preferentially along grain boundaries, causing shunt paths and forming donor defects [25]. This AST proves that also Se causes instability, depending on its concentration. This does not appear to be due to an actual diffusion of selenium during the AST since the most unstable sample is 400/400, where the CdSeTe compound is already homogeneous throughout the thickness, and, therefore, the diffusion coefficient of Se should be minimal. One hypothesis could be that some defects formed by selenium are not stable and tend to change nature over time, as had already been seen for copper, where the decay of the acceptor Cu_{Cd} into the acceptor-donor pair Cu_i-V_{Cd} was observed [25].

On the other hand, this significant degradation of the devices could also be due to the copper itself since a higher concentration of selenium leads to the formation of smaller grains throughout the absorber, increasing the amount of grain boundaries and thus favouring the diffusion of Cu from the back contact towards the junction. Furthermore, in a thicker absorber, the reduction in the amount of copper at the back contact over time (due to its diffusion) leads to the roll-over effects, causing a decrease in FF. However, this effect is much less noticeable for thin absorbers where the space charge regions at the p–n junction and at the back contact tend to overlap [26].

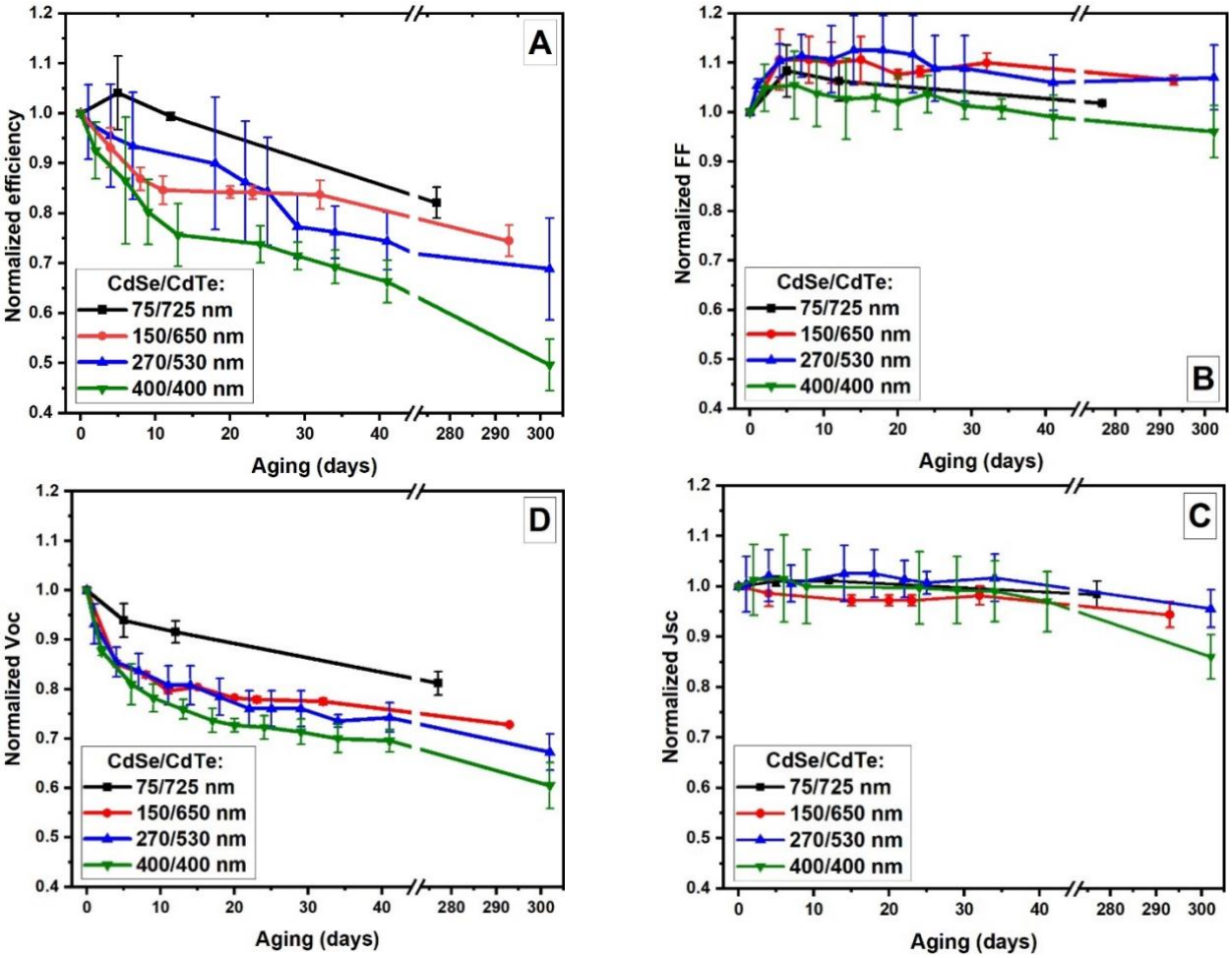

Figure 9.12: Graphs reporting the performance degradation along time of the different CdSe/CdTe ratios samples. Normalized efficiency (A), FF (B), Jsc (C) and Voc (D) values at various time steps of AST.

9.5 Conclusions

CdSeTe/CdTe devices with reduced absorber thickness of 0.8 µm with different CdSe/CdTe ratios have been fabricated to study the impact of selenium concentration in ultra-thin absorbers. Thinning the absorber thickness has the advantage of reducing costs, material availability, and environmental effects; thus, it is now essential to understand the impact of selenium introduction in ultra-thin absorbers.

Interestingly, in these cells, there is no evidence of the CdSeTe/CdTe bi-layer structure observed in devices with thicker CdTe; here, selenium diffuses throughout the entire absorber, even using 75/725 nm of CdSe/CdTe. With this ratio, SIMS analysis suggests the formation of a graded band gap, with a decreasing concentration of Se towards the back contact; even if the hyperspectral CL map shows that the band gap of the absorber mainly changes from grain to grain, thus also parallel to the substrate. By increasing the CdSe/CdTe ratio, the measurements show a progressive reduction of the minimum band gap and an increase in the net charge density, thus demonstrating the insertion of Se into the lattice structure and its function of passivation of the grain boundaries. Furthermore, enhancing the net charge density narrows the depletion region width, a factor that should not be neglected given the thin absorber thickness; a completely depleted absorber leads to increased recombination in the back contact region.

On the other hand, by increasing the selenium concentration, a progressive decrease in grain size occurs along the entire thickness of the absorber. It is, therefore, not limited to the junction region alone. This inevitably increases the amount of grain boundaries and, hence, the possible carrier recombination. Using a CdSe/CdTe ratio of 1/1, a structure composed of small, disorderly-arranged grains is formed, with also the presence of voiding. This results in a marked reduction in quantum efficiency for all wavelengths and, consequently, a drop in device performance.

Selenium introduction also affects the stability of the devices: accelerated stability tests prove that by increasing Se concentration, the stability of the cells reduces, mainly due to the degradation of Voc.

The 150/650 nm CdSe/CdTe samples fabricated without Br-MeOH etching demonstrate the best compromise between the effects of the selenium introduction mentioned above, leading to the highest performances. Currently, in our laboratory, these samples have reached a remarkable (considering the ultra-thin absorber) efficiency of 12.8 %.

The different Se concentrations in different grains have been attributed to the energetically favorable diffusion of Se through specific crystal orientations of CdTe compared to others. In a 2-3 µm thick as-deposited CdTe, a few layers of grains form the film thickness; thus, while diffusing through the grain boundaries, Se can surround the grains of the first layer/layers and enter through the preferred orientation into the matrix. On the other hand, if the grains extend throughout the entire thin thickness of the as-deposited CdTe, Se is disadvantaged during the activation treatment in accessing some grains, depending on their orientations. Moreover, starting from a CdTe film composed of a single layer of grains, it is impossible to obtain a CdSeTe/CdTe bi-layer; this limits the grain size growth throughout the absorber.

9.6 References

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Chapter 10

Oxygen-Passivated Interrupted Growth and Oxygen-Free Continuous Growth: A Comparative Study of CdSeTe Absorbers Growth

*** The work presented in Chapter 10 & 11 was conducted at the CTF facilities as part of my PhD mobility program. The devices were fabricated at CTF Solar GmbH, during my PhD mobility. The concept of the work presented in these chapters were introduced by Dr. Robert Arndt and his team. I had the opportunity to stay at CTF for 6 months having the chance to take part in the experiments and to work with their facilities.**

10.1 Introduction

The incorporation of CdSeTe alloys into CdTe-based thin-film solar cells has enabled power conversion efficiencies exceeding 23% through effective bandgap engineering and enhanced long-wavelength absorption. Despite this progress, the role of oxygen during CdSeTe deposition remains insufficiently understood, as most reported close-spaced sublimation (CSS) processes are intentionally oxygen-free. Specifically, regulating alloy composition during CSS development is more difficult by the intrinsically differing sublimation and evaporation rates of CdSe and CdTe. In this study, we examine the effects of oxygen incorporation on microstructure, defect passivation, and device performance in CdSeTe non-graded absorbers. Both absorbers were deposited as multilayer stacks. One absorber included an intentional vacuum break between layers, which is assumed to result in oxygen incorporation, whereas the other absorber was deposited continuously without a vacuum break.

Despite smaller grains (~0.5 µm), the oxygen-containing absorber yields a better device efficiency (12.9%) than the oxygen-free absorber (9.1%), which displays massive grains (>1.7 µm). This unexpected behavior is explained by the incorporation of oxygen during vacuum breaks, which interacts with the different evaporation rates of CdSe and CdTe and alters the incorporation of selenium during fabrication. Increased open-circuit voltage (~660 mV) and shunt resistance are the results of the integrated oxygen segregation to grain boundaries and interfaces, where it passivates defects and suppresses shunt pathways.

On the other hand, the oxygen-free absorber exhibits large grain growth and extensive recrystallization during $CdCl_2$ activation, but it has poor voltage (~580 mV) and fill factor due to lack of effective passivation and voids are created by interdiffusion. These results show that oxygen added during interrupted growth functions as a passivant that influences alloy formation

during deposition and can partially compensate the microstructural defects in undoped CdSeTe absorbers.

Overall, this study highlights the critical interplay between oxygen, deposition method, and the intrinsic differences in CdSe and CdTe sublimation behavior, providing insight into how oxygen assisted processes can be leveraged or intentionally avoided in the transition toward stable, intentionally doped, high-efficiency CdSeTe solar cells.

Oxygen is often considered a detrimental impurity in the larger framework of semiconductor physics. Oxygen incorporation usually results in the creation of deep-level traps that function as non-radiative recombination sites in single-crystal silicon (Si) [1] and gallium arsenide (GaAs) [2], significantly reducing the lifetime of minority carriers. However, in polycrystalline CdTe, the grain boundaries (GBs) are locations of significant structural disturbance and frequently contain a high density of voids and dangling bonds [3].

The CdTe community has understood that oxidation to some extent is advantageous. It has been demonstrated that adding oxygen during the $CdCl_2$ activation treatment, increases carrier density and passivates grain boundaries [4]. However, the function of oxygen in the actual sublimation growth is still unclear. Does the inclusion of oxygen into the bulk film during growth function as a defect generator, a dopant, or a passivation?

Our research investigates this by identifying the effect of vacuum interruption. We examine oxygen's complex role by comparing Interrupted Deposition, which introduces oxygen layers throughout the film stack, to Continuous Oscillation (DX), which maintains a clean high-vacuum environment. This research will examine the physical, chemical, and electrical ramifications of this oxygen transition to better understand why physically superior crystals/larger grains can result in electronically poor devices performance.

10.2 Device Fabrication

$CdSe_xTe_{1-x}$ /CdTe devices are fabricated in superstrate configuration by close space sublimation (CSS) having a total thickness of 2µm. The device was fabricated at CTF Solar GmbH, during my PhD mobility. The concept and idea of the work presented in this chapter is developed by Dr. Robert and his team and I had a chance to be a part of their experiments.

I would like to specifically acknowledge **Dr. Pascal** and **Mr. Sagar** for their invaluable scientific and technical guidance during the execution of my experiments. Their support was instrumental in the systematic labeling of samples and the subsequent data analysis and visualization using Minitab and Igor Pro.

10.2.1 Interrupted Multilayer Deposition

The Interrupted Multilayer Deposition was performed using a top-down CSS tool located at CTF. This specific configuration utilizes directed sublimation gas transport to the substrates. The source consists of two distinct units one CdSe and one CdTe allowing for the alternating deposition of strata.

The tool is designed for high-throughput batch processing, accommodating substrate sizes up to 30 × 40cm. It supports various operational modes, including continuous operation and oscillation mode. The absorber is fabricated as layers of alternating CdSe and CdTe strata rather than as a single continuous layer. This method is distinguished by the evacuation of the substrates from the vacuum chamber between layer depositions (shown in Figure 10.1) to precisely control the layer transitions and facilitate the atmospheric exposure required to differentiate between air-exposed and air-absent absorbers.A discontinuous, confined growth phase is represented by the oxygen exposed absorbers (ODX) protocol.

The semiconductor surface is exposed to a strong flux of oxygen (O_2), nitrogen (N_2), and water vapor (H_2O) when it is removed from the vacuum chamber ($<10^{-5}$ Torr) and placed in ambient air. Chemisorption happens nearly instantly due to the strong reactivity of tellurium and cadmium surfaces. When oxygen molecules adsorb onto surface sites, they most likely interact with surface dangling bonds to generate Cd-O or Te-O links or build sub-monolayers of oxides like CdO or TeO_2.

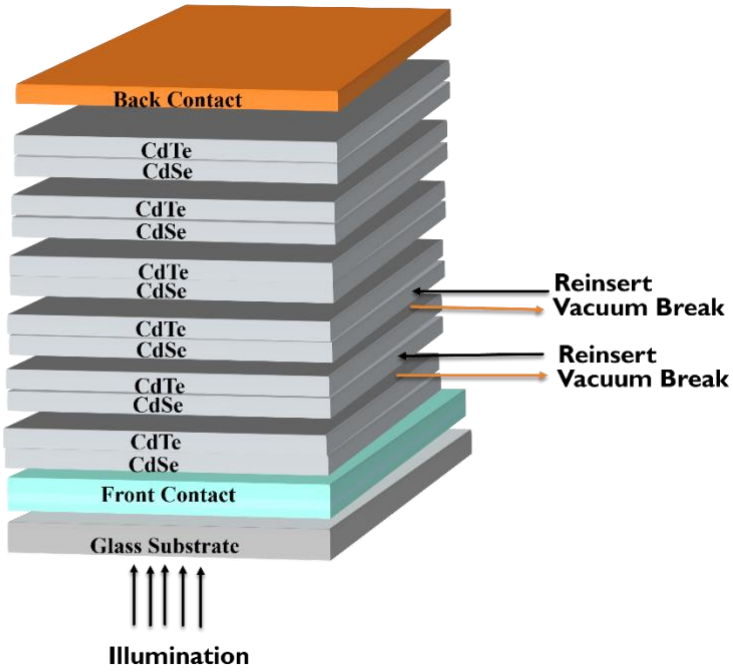

Figure 10.1: Device configuration of Interrupted Multilayer (ODX) Absorber

The substrate is repeatedly heated and cooled during the extraction and re-insertion processes. This heat shock has the potential to cause stress and affect the subsequent layer's nucleation density.

The resulting stack is uneven, with the interface between the CdSe and CdTe layers mediated by a thin, disordered layer of oxides rather than a clean stack.

10.2.2 Continuous Oscillation Deposition (DX)

The DX represents the high-vacuum growth method. In this method, the substrate oscillates mechanically between the CdSe and CdTe sources without breaking the vacuum.

Throughout the whole deposition process, the background pressure is kept at a high vacuum ($<10^{-5}$ Torr). The only factor limiting the partial pressure of oxygen is the chamber's residual gas background.

The substrate remains at the growth temperature (500-550^{o}C) during the entire absorber deposition process. Due to the differences in these approaches, two different types of materials are produced: the DX films are monolithic alloys, and the ODX films are essentially oxide-pinned composites.

10.3 Study of absorber layer

10.3.1 Microstructural Analysis

A fundamental concept of polycrystalline photovoltaic material research is that bigger grains are preferred. Grain boundary has a lower volume fraction when the grains are large. Reducing grain boundaries should increase carrier lifetime and open-circuit voltage (Voc) because they are usually areas of high defect density, non-radiative recombination and impurity segregation [5]. This is strongly related to our experiment which shows a performance inversion where higher efficiency is correlated with smaller grains.

To understand the morphology at cross-sectional scanning electron microscopy (SEM) was used on the cross section of as deposited absorber and the treated absorber. The cross section of the as deposited sample clearly revels the multiple layer stack of CdSe and CdTe as shown in Figure 10.2 (A), with very high roughness and some porosity.

The SEM results for the absorber after activation treatment reveals complete Se-Te interdiffusion and recrystallization. The grains are small, with average lateral dimensions restricted to approximately 0.5 µm as shown in figure 10.2 (B).

The primary driver for this restricted growth is the presence of the oxidized interfaces introduced during vacuum interruptions. As the film undergoes the $CdCl_2$ activation treatment, activation residues (cadmium-oxide-chloride) are partially embedded into the absorber.

10.3.2 Morphology of Oxygen-Containing Absorbers

To understand the morphology the Cross-sectional Scanning Electron Microscopy (SEM) was used on the cross section of as deposited absorber and the treated absorber. The cross section of the as deposited sample clearly revels the multiple layer stack of CdSe and CdTe as shown in Figure 10.3(A), with very high roughness and some porosity for ODX absorber.

The SEM results for the absorber after activation treatment at 450 ^{o}C for 15 minutes reveals complete Se-Te interdiffusion and recrystallization. The grains are small, with average lateral dimensions restricted to approximately 0.5 µm as shown in figure 10.3 (B).

The primary driver for this restricted growth is the presence of the oxidized interfaces introduced during vacuum interruptions. As the film undergoes the $CdCl_2$ activation treatment, activation residues (cadmium-oxide-chloride) are partially embedded into the absorber.

10.3.3 Morphology of Oxygen-Free Absorbers

In contrast, the DX films grown under continuous vacuum with the oscillation of substrate between the CdSe and CdTe source. The SEM results of as deposited absorber show epitaxial growth of second CdSe layer with a formation of high porosity below second CdSe layer caused by interdiffusion and volume contraction.

After a weak activation treatment, we see a complete Se-Te interdiffusion with a grain growth of lateral size of 0.9 µm having a cadmium-oxide-chloride activation residues mainly on the surface of the absorber. With a strong activation treatment, the absorber exhibits massive recrystallization with a complete Se-Te interdiffusion having a large grain growth (lateral size 1.7 µm). Activation residues (cadmium-oxide-chloride) are seen on the absorber surface and partially incorporated into the absorber.

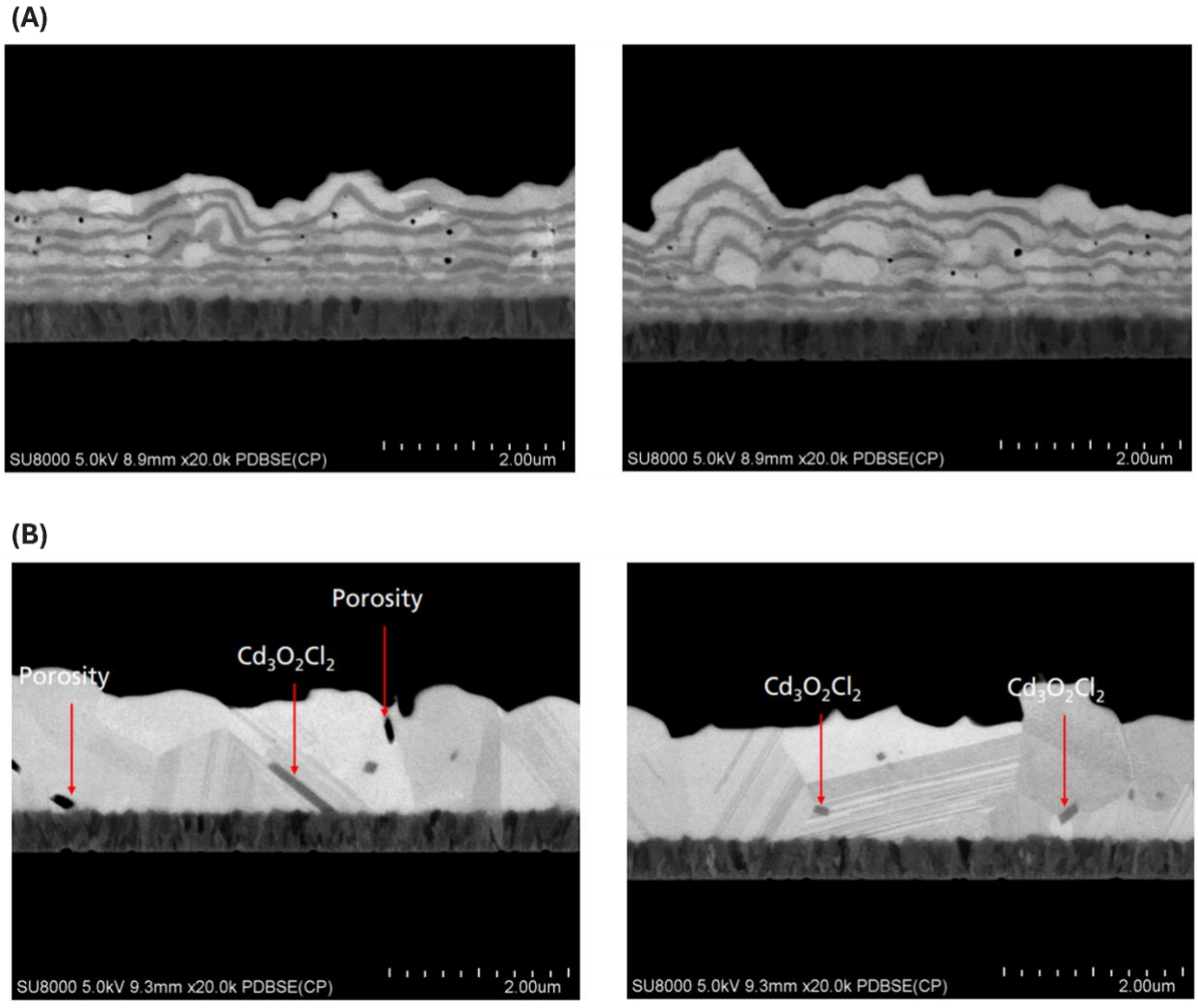

Figure 10.2: Cross-sectional of Scanning Electron Microscopy (SEM) images of Oxygen-containing Absorber (ODX) (A) As deposited absorber (B) Activated absorber

The resulting grains possess lateral dimensions exceeding 1.7 µm, more than three times the volume of the ODX grains.

While interdiffusion of tellurium and selenium occurs within the $CdSe_xTe_{1-x}$ system, the scale of post-deposition diffusion is insufficient to fully account for the observed porosity via the Kirkendall effect [6] in these ultra-thin layers. Instead, the formation of voids is more likely driven by lattice contraction. When the substrate enters the significantly hotter CdSe deposition area, the initial CdTe layer undergoes a rapid thermal adjustment. This lattice shrink likely triggers the formation of voids, with grain boundaries serving as the primary nucleation sites for the resulting

porosity [7]. The SEM cross-sections of the DX absorber clearly show these voids as subsurface porosity.

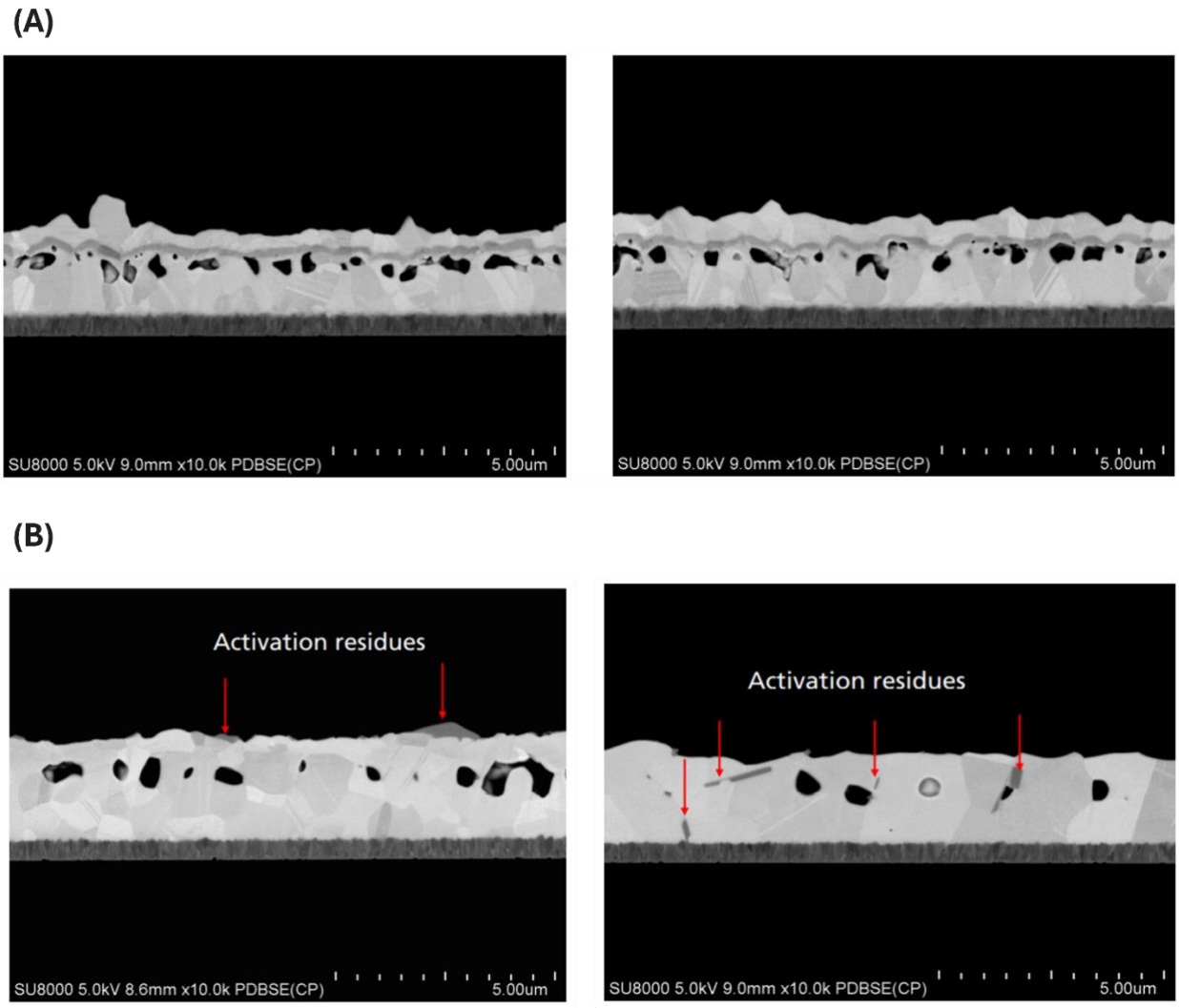

Figure 10.3: Cross-sectional of Scanning Electron Microscopy (SEM) images of Oxygen-Free Absorber (A) As deposited absorber (B) Activated absorber

Kirkendall void formation has a negative effect on solar cell performance. Within the absorber, a void essentially generates a new internal surface. These internal void surfaces are chemically active and serve as strong recombination sinks for minority carriers, in contrast to the external surfaces, which can be passivated [8]. Voids increase the device's series resistance by decreasing the effective cross-sectional area for current transfer.

If the voids are large enough or interconnected, they can move the back-contact metals (like gold or copper) toward the junction, creating localized shunts that degrade fill factor (FF). [8]

In the ODX films, the oxide layers formed at the interfaces likely play a protective role by physically impeding the interdiffusion of Se and Te. However, the superior film quality may also be attributed to the mitigation of thermal shock during growth. Unlike the continuous process, the ODX protocol involves growth conditions that appear to reduce frequent thermal stress, preventing the lattice-shrinkage and subsequent void formation observed in oxygen-absent samples. This combination of a chemical diffusion barrier and stabilized thermal conditions lead to a more coherent interface.

The disordered nature of the oxidized interface and the high density of grain boundaries in ODX films provide sinks for vacancies. Vacancies can be absorbed at these defects rather than coalescing into voids.

The ODX films, despite having vacuum break, maintain better structural integrity. The oxide contamination prevents the formation of Kirkendall voids, preserving the continuity of the material at the expense of grain size.

10.3.4 Defect Chemistry and Atomic-Level Passivation

The physical analysis establishes that ODX films are fine grained and void free, while DX films are large-grained but void-prone. However, the magnitude of the efficiency gap (12.9% vs 9.1%) cannot be explained by voids alone. The dominant factor is the electronic quality of the grain boundaries themselves.

In CdTe, grain boundaries are complex dislocations that interfere with the lattice's periodic potential.

The cadmium and tellurium atoms have dangling bonds and unsaturated orbitals due to the sudden termination of the crystal lattice at a grain boundary. In particular, deep trap states are produced close to the middle of the bandgap by tellurium-tellurium (Te-Te) atoms and cadmium vacancies (V-Cd) at the boundary.

Shockley-Read-Hall (SRH) statistics show that these mid-gap states function as extremely effective recombination centers Instead of allowing electrons and holes to be captured as current, they capture them, allowing them to recombine and be lost as heat. This results in a severe pinning of the Fermi level, which restricts the open-circuit voltage (Voc), and a decrease in the lifetime of minority carriers [9].

The research shows that ambient oxygen functions as an effective passivant for these grain boundary flaws. Instead of staying in the interior of the grain, oxygen has a strong thermodynamic

propensity to segregate to the grain borders [10]. The chemical affinity of oxygen for tellurium and cadmium as well as the relaxation of lattice strain are the driving forces behind this segregation.

Oxygen atoms interact chemically with the dangling bonds when they occupy sites near the grain border. For instance, oxygen can produce oxidized atoms (such as TeO_3^{2-} complexes) by bonding with Te dangling bonds. According to first-principles density functional theory (DFT) computations [3], [11], this bonding reduced the bandgap. The Te-Te dimers deep levels are either removed or driven to the band boundaries, where they transform into shallow states that are less detrimental to carrier lifespan.

The film is effectively doped with oxygen at regular intervals during the ODX deposition process. These oxygen vessels become absorbed into the film's structure as it activated. The high density of boundaries in the ODX film is successfully passivated during the subsequent activation anneal because oxygen diffuses quickly along the grain boundary [12]. This leads to a material that is electrically good but physically defective (many boundaries).

The DX films, on the other hand, are developed under a high vacuum environment. Despite the fact that the DX films contain huge grains and consequently fewer grain boundaries. They continue to have a high density of dangling linkages at deep levels.

As a result, there is a very high surface recombination velocity at these boundaries. The device performance is dominated by the high recombination rate at these active defects, which lowers the Voc to about 580 mV as opposed to about 660 mV for the passivated ODX films.

Another passivant, chlorine, is introduced via the $CdCl_2$ activation treatment. The better performance of the ODX films, however, indicates that chlorine is not enough to completely passivate the flaws in the materials. For undoped absorbers to perform at their best, a synergistic effect appears to be required, where oxygen passivates certain flaws that chlorine cannot.

In addition to passivation, oxygen helps to determine the absorber's doping concentration.

Oxygen incorporation has been linked to an increase in net acceptor density in CdTe, but it is not a shallow acceptor like arsenic. This could result from direct isoelectronic substitution effects that change the Fermi level position or via the development of complexes that stabilize cadmium vacancies, which are acceptors [12].

In contrast to ODX films, the DX samples exhibit a lower p-type carrier density, likely due to the presence of structural voids as previously discussed. This reduction in carrier concentration weakens the built-in electric field at the p-n junction. Conversely, the optimized carrier density in ODX films contributes to the significantly higher measured Voc (660 mV) and facilitates more efficient separation of photo-generated carriers.

10.4 Electrical Performance

When the electrical performance of the devices was compared, an unexpected result yield: structurally superior DX films performed much worse than microstructurally limited ODX films.

The most significant parameter for DX absorber is their 80mV Voc deficiency. The ratio of light-generated current to saturation current is logarithmically related to Voc. Recombination activity is directly measured by the saturation current.

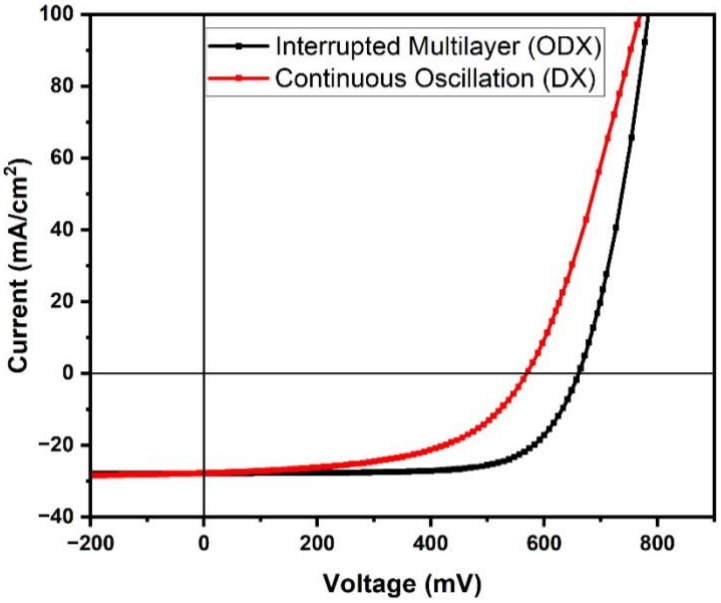

Figure 10.4: Jv analysis of Oxygen containing (ODX) and Oxygen free (DX) absorbers

Due to SRH recombination at the un-passivated grain boundaries and the internal surfaces of Kirkendall voids, the low Voc in DX films suggests a significant rise in saturation current. Because the boundaries are electrically inactive, the ODX films have a lower overall recombination rate even though they have a larger grain boundary area.

The low shunt resistance and fill factor in DX films are consistent with voids.

Massive, linked voids can provide as pathways for back-contact metals to diffuse toward the junction, resulting in partial leakages. On the other hand, resistive oxide inter-layers are present in the ODX films. These oxides primarily limit shunt routes, while they may also raise series resistance. By creating a complicated path for any leakage current, the ODX absorber efficiently protects the device from pinholes.

The study concludes that ODX is a better approach for undoped or Cu-doped device since it uses oxygen as a coincidence passivant. But ODX is essentially limited. Because of the small grain size, carrier mobility and longevity are limited, which will ultimately limit efficiency to 18–19%. We need to use the large grains of the DX mode in order to attain the theoretical limitations (>25%).

10.5 Conclusion

This study highlights the role of oxygen incorporation in the fabrication of close-spaced sublimation (CSS) processed CdSeTe absorbers. Despite having much smaller grains (~0.5 µm vs. >1.7 µm), our results show that oxygen-exposed absorbers achieve superior device efficiency (12.9%) compared to their oxygen-free counterparts (9.1%), disregarding conventional assumptions that maximize grain size is the primary driver of performance.

The ODX absorber performance is attributed to the segregation of oxygen to grain boundaries and interfaces, where it functions as an effective passivant. This mechanism reduces non-radiative recombination and suppresses shunt pathways, leading to a marked improvement in open-circuit voltage (~660 mV) and shunt resistance. Conversely, the oxygen-free process, while having extensive grain growth, suffers from reduced voltage (~580 mV) and fill factor due to un-passivated defects and the formation of voids driven by the differing sublimation rates of CdSe and CdTe.

Ultimately, these findings highlight that microstructural size is secondary to electronic quality in CdSeTe absorbers. We conclude that controlling oxygen exposure during deposition is a vital lever for optimizing alloy composition and defect management, offering a strategic pathway to enhance the stability and efficiency of next-generation CdSeTe thin-film solar cells.

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Chapter 11

Study of Oxygen Impact on the of Activation Treatment of Arsenic-Doped CdTe Solar Cells

***The work presented in Chapter 10 & 11 was conducted at the CTF facilities as part of my PhD mobility program. The devices were fabricated at CTF Solar GmbH, during my PhD mobility. The concept of the work presented in these chapters were introduced by Dr. Robert Arndt and his team. I had the opportunity to stay at CTF for 6 months having the chance to take part in the experiments and to work with their facilities.**

11.1 Introduction

This study investigates the impact of $CdCl_2$ activation atmospheres on the photovoltaic performance of arsenic-doped cadmium telluride (CdTe: As) solar cells. Using (Tech12D/CdTe) with a fixed absorber thickness of 2µm. We performed a comparative analysis of CdTe: As absorbers activated in ambient air versus an inert nitrogen (N_2) environment. While standard air activation proved detrimental to the doped samples, resulting in a degradation of efficiency to 14.35% due to dopant deactivation, activation in a nitrogen atmosphere successfully unlocked the potential of the Group V dopant. The nitrogen-activated devices achieved a champion efficiency of 17.11%, significantly outperforming both the air-activated doped samples and the intrinsic CdTe control (16.2%). This performance enhancement is driven by a substantial increase in Open Circuit Voltage (Voc~850mV) and Fill Factor (77.4%), supported by a doubling of the Shunt Resistance (>3300 $\Omega.cm^2$). External Quantum Efficiency (EQE) analysis confirms a sharp absorption edge at 840nm, indicating that the nitrogen atmosphere preserves the phase purity of the CdTe absorber without introducing optical losses. These findings establish that inert atmosphere activation is a critical processing step for maximizing the efficiency of Arsenic-doped CdTe photovoltaics.

To date, high-efficiency CdTe devices have primarily relied on Copper (Cu) doping to form the p-type absorber. However, Cu-doped CdTe technology faces fundamental limitations. The hole density in Cu-doped absorbers typically saturates at the low 10^{14} cm^{-3} range due to self-compensation mechanisms and the formation of compensating defects [1]. Furthermore, Copper is a fast diffuser in the CdTe lattice, which poses long-term stability risks due to dopant migration toward the front junction under operating conditions [2].

To overcome the voltage deficit (Voc) associated with low carrier concentration, recent research efforts have shifted toward Group V elements (Phosphorus, Arsenic, Antimony) as substitutional p-type dopants. Theoretical calculations and initial experimental results suggest that substituting

tellurium sites with Group V atoms (As_{Te}) can yield hole densities exceeding $10^{16}cm^{-3}$ and minority carrier lifetimes greater than 20ns [3], [4]. Metzger et al. recently demonstrated polycrystalline CdTe solar cells doped with arsenic achieving efficiencies of 20.8%, validating the potential of this doping strategy [4], [5]. However, the transition from Cu to Group V doping necessitates a re-evaluation of the standard $CdCl_2$ activation process. The activation step, typically performed at high temperatures (400-450 ^oC), is critical for recrystallization, grain growth, and grain boundary passivation. In conventional Cu-doped devices, this process is invariably conducted in an oxygen-containing atmosphere (Air), as oxygen is known to assist in stacking fault removal and chemically passivate grain boundaries [5], [6]. For arsenic-doped absorbers, the role of oxygen is more complex and potentially detrimental. Recent studies indicate that oxygen can react with arsenic dopants to form insulating oxides (e.g., As_2O_3) or deep-level defects rather than the desired shallow acceptor states [7]. This oxidation can deactivate the dopant, leading to Fermi level pinning and reduced device performance. Consequently, inert atmospheres such as Nitrogen (N_2) or Argon have been proposed to prevent dopant oxidation while maintaining the benefits of recrystallization [8], [9]. Despite these insights, a direct comparative study isolating the effect of activation atmosphere on 2µm thick As-doped absorbers while maintaining a standard Cu-back contact process remains limited in the literature. This study addresses this gap by systematically comparing the photovoltaic performance of arsenic-doped CdTe activated in air versus nitrogen. We demonstrate that while air activation degrades the performance of doped absorbers, activation in a nitrogen environment successfully unlocks the doping efficiency, yielding devices with efficiencies exceeding 17%, high fill factors, and improved voltage stability compared to intrinsic CdTe absorber.

11.2 Device Fabrication

At CTF Solar GmbH, the thin film was deposited on commercial glass substrates, followed by fabrication of the absorber layer via close-space sublimation in a superstrate configuration as shown in figure 11.1. The absorber thickness was 2 µm.

I would like to specifically acknowledge **Dr. George** and **Dr. Pascal** for their invaluable scientific and technical mentorship. Beyond their guidance in executing the experiments, their insights into the underlying physics and chemistry were fundamental to my understanding. I especially appreciate their support in solving complex challenges and for their help in defining the next step throughout the research process.

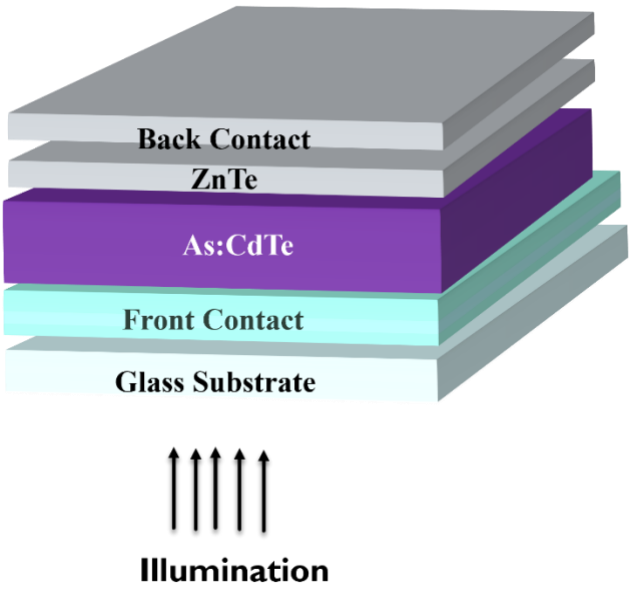

Figure 11.1: Device Configuration Fabricated and analyzed

Later, the activation treatment is applied by drop-casting a $CdCl_2$-methanol solution on the surface and subsequently annealing in air and nitrogen at 420 ^oC. Following this, the samples were etched in a diluted HCL solution, which removes the $CdCl_2$ residuals from the surface. Then the Cu dopped ZnTe was deposited using thermal evaporation method. Then the sample goes through from FRP and laser scribing. Finally, we deposit the back contact and the sample undergoes an air annealing at 230 °C to complete the device stack. The area of each cell is 1 cm^2.

11.3 Results and Discussion

Photovoltaic Performance (J-V Characteristics)

The intrinsic CdTe sample activated in standard air conditions, show a high-performance baseline with an efficiency of 16.24% and a Voc of 826 mV. However, the introduction of Arsenic doping followed by standard air activation (As: CdTe-Air) resulted in a significant deterioration of device performance (14.35%) as shown in Table I. This degradation is primarily driven by a drop in Voc to 789mV and a severe reduction in Fill Factor (70.98%). This behavior is consistent with recent literature suggesting that oxygen, while beneficial for intrinsic CdTe, acts as a detrimental impurity for Group V doped absorbers. High-temperature processing in air promotes the formation of Arsenic oxides (e.g., As_2O_3) or AsO complexes at grain boundaries, which act as deep-level non-radiative recombination centers rather than shallow acceptors [1], [2].

Table 11.I: peak efficiency parameters of samples fabricated in air and nitrogen.

Absorber	$CdCl_2$ Activation	FF [%]	Voc [%]	Jsc [mA/cm^2]	Eff [%]
CdTe	Air	76.6	825.7	25.7	16.2
As:CdTe	Air	71	789.2	25.6	14.3
As:CdTe	Nitrogen	77.5	849.9	26	17.11

In contrast, activating the As-doped absorber in an inert Nitrogen atmosphere (As: CdTe-N) yielded a substantial performance boost, achieving a champion efficiency of 17.11% as shown in figure 2. This represents a notable improvement over both the air-activated doped sample and the intrinsic control. The Voc increased to 850 mV, an improvement of ~25mV over the reference CdTe cells. This voltage enhancement confirms the successful incorporation of arsenic on tellurium sites (As_{Te}), which increases the net hole density (p) and reduces the Fermi-level splitting deficit (Voc deficit), as predicted by defect thermodynamics models [3], [4].

The influence of the activation atmosphere is most visible in the Shunt Resistance (Rsh) and fill factor data. The As: CdTe-Air samples exhibited a low Rsh of ~ 1150 Ω.cm^2, indicating significant leakage currents. This supports the hypothesis that oxidation of the dopant creates conductive pathways or shunting defects along the grain boundaries [5]. Conversely, the As: CdTe-N samples achieved the highest Rsh of ~3323 Ω.cm^2, nearly doubling the value of the intrinsic control (~2176 Ω.cm^2). This indicates that the nitrogen atmosphere not only prevents dopant oxidation but also facilitates effective grain boundary passivation, likely through the formation of benign As-rich grain boundary chemistries that block minority carriers' recombination [6]. The combination of high R_{sh} and reduced series resistance (R_s) contributed to a high fill factor of 77.4%, demonstrating that the transport properties of the 2µm absorber are not compromised by the absence of oxygen during activation.

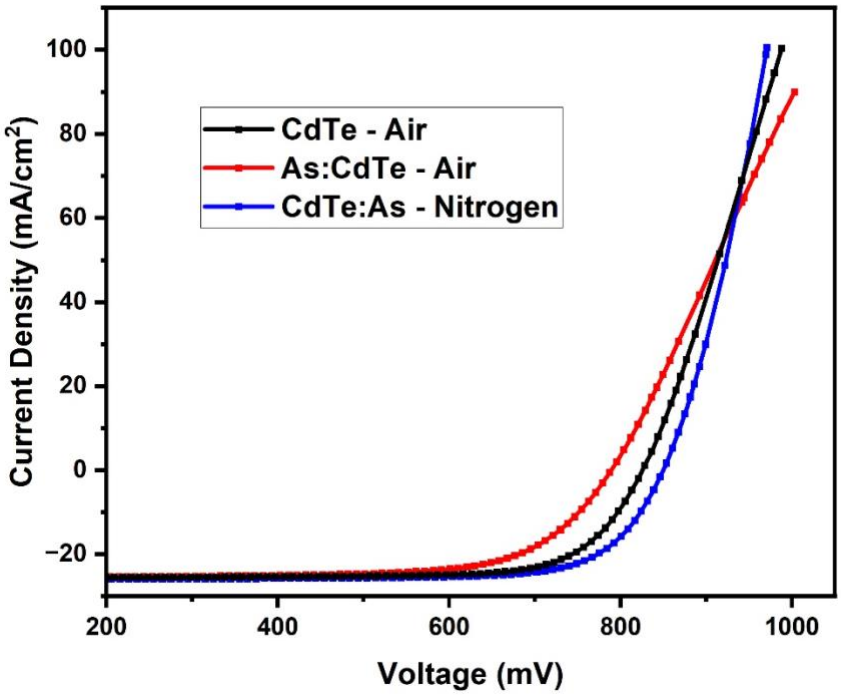

Figure 11.3: JV curves of the samples fabricated in different activation atmospheres.

A common challenge reported in Group V doping studies is a reduction in short circuit current (J_{sc}) due to reduced grain size or bulk lifetime degradation when switching from air to inert activation atmospheres [8], [9]. However, our results show no such trade-off. The External Quantum Efficiency (EQE) spectra (Figure 11.3) reveal that the Nitrogen-activated devices maintained a high Jsc of 26.01 mA/cm^2, slightly surpassing the reference CdTe cell (25.68 mA/cm^2).

The EQE cutoff at ~ 840 nm (~1.48eV) confirms that the bulk phase purity of CdTe is preserved [10] in the Nitrogen process. The high and flat EQE response in the visible region (500-800 nm) indicates excellent minority carrier collection length (L_d). This implies that the diffusion length in the As-doped/Nitrogen-activated grains is sufficiently large to collect carriers across the full 2µm absorber thickness, negating the need for oxygen-assisted grain growth typically required in undoped devices.

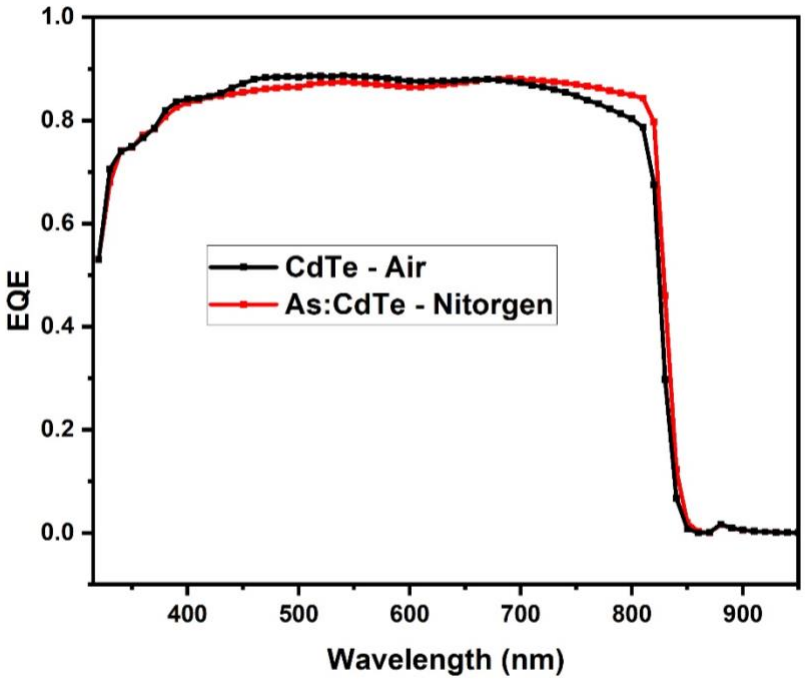

Figure 11.4: EQE Spectra of device activated in different atmosphere.

11.4 Conclusion

This study systematically evaluated the influence of activation atmosphere on the performance of 2µm thick arsenic-doped cadmium telluride (As: CdTe) solar cells. By comparing standard air activation with inert nitrogen processing, we demonstrated that the activation environment is the critical determinant for successfully leveraging Group V dopants. Our results indicate that standard air activation is incompatible with Arsenic doping, leading to dopant deactivation and a significant reduction in device performance (~14.35%). In contrast, activation in a nitrogen atmosphere successfully prevented dopant oxidation, unlocking the full potential of the Arsenic acceptor. The nitrogen-activated devices achieved a champion efficiency of 17.11%, effectively outperforming the intrinsic CdTe control (16.24%). This performance boost was driven by a concurrent increase in Open Circuit Voltage (Voc~850 mV) and Fill Factor (77.4%), supported by a doubling of the shunt resistance (>3300 $\Omega.cm^2$). Crucially, this study highlights a no-compromise regime for As-doped CdTe unlike literature reports where inert activation often degraded carrier collection, our optimized nitrogen process maintained a high short circuit current (Jsc~26 mA/cm^2) comparable to the air-activated CdTe cell. We conclude that inert atmosphere activation is essential for realizing high-efficiency, As-doped CdTe photovoltaics, providing a viable pathway to exceed the performance limits of standard copper-doped technologies.

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Chapter 12

Analysis of Bifacial CdTe Top Cells for CdTe/Si Tandem Applications

12.1 Introduction

Crystalline silicon solar cells are rapidly approaching their theoretical Shockley-Queisser efficiency limit of around 30% [1], which will prevent further major increases in single-junction technology. To overcome this obstacle tandem setups combining a silicon bottom cell and a wide-bandgap top cell are required [2]. Among these, CdTe/Si tandems present a commercially scalable and possibly more stable substitute for perovskite-based devices [3]. The fabrication of a transparent back contact (TBC) for the CdTe top cell that enables sub-bandgap light to reach the bottom cell without compromising electrical performance is a crucial obstacle to the development of this technology.

This paper focuses on the fabrication and optimization of bifacial CdTe solar cells with RF-sputtered Indium Tin Oxide (ITO) as a transparent back contact. We investigated the impact of copper layer thickness, optimized the Indium Tin Oxide (ITO) thickness, and compared the Indium Tin Oxide (ITO) with gold (Au) as back-contact materials.

The optimized device, utilizing a 1 nm copper having thicker (10 minutes) ITO layer deposition, achieved a front-side efficiency of 10.2%, comparable to the 10.5% efficiency of standard opaque gold-contact devices. Most importantly, the device showed full bifacial performance with a fill factor of 64% and an efficiency of 2.56% under rear illumination, it confirmed effective carrier extraction regardless of light direction. The 2 µm absorber thickness prevents carriers generated on the back surface from reaching the front p-n junction, which accounts for the notable difference in short-circuit current (23 mA/cm² front vs. 6 mA/cm² rear). With a transparency onset near 850 nm, the optimized device demonstrates the necessary spectral filtering capabilities for 4-terminal CdTe/Si tandem configurations.

The global transition toward renewable energy necessitates photovoltaic (PV) technologies that reaching the theoretical efficiency limits of single-junction devices. While crystalline silicon (c-Si) dominates the current market with a share exceeding 95%, its practical efficiency is approaching the detailed-balance Shockley-Queisser (SQ) limit of approximately 30% [1]. To achieve the US Department of Energy's (DOE) 2030 targets for levelized cost of electricity (LCOE), the next generation of solar modules must routinely deliver efficiencies exceeding 30% [2]. Tandem solar

cell structure, which stack absorbers with complementary bandgaps to minimize thermalization losses, offer the most viable pathway to this goal.

Among the various tandem configurations, the pairing of a wide-bandgap cadmium telluride (CdTe) top cell with a c-Si bottom cell represents a strategic, stability-oriented alternative to the more widely publicized perovskite-silicon tandems [3]. While perovskites have demonstrated rapid efficiency gains recently achieving 34.85% in tandem configurations [4], they remain plagued by intrinsic instability, moisture sensitivity, and toxicity concerns that complicate bankability [5]. In contrast, CdTe is a proven, commercialized thin-film technology with a multi-gigawatt manufacturing base, demonstrated field reliability, and a theoretical efficiency potential that, when coupled with silicon, exceeds 32% [6].

This research provides the analysis of the bifacial CdTe/Si tandem device by pairing a ~1.5 eV CdSeTe top cell with a 1.12 eV silicon bottom cell, focusing on the critical role of bifacial device as both the semitransparency required for spectral splitting and the capability to harvest albedo radiation. We analyze the materials science of Indium Tin Oxide (ITO) as a transparent back contact (TBC) for hole extraction and its integration with graded CdSeTe/CdTe absorbers.

12.1.1 Bifacial CdTe and Silicon Tandem structure

Photovoltaic technology is increasingly focused on tandem devices capable of exceeding the efficiency of a single-junction crystalline silicon (c-Si) solar cell. As silicon is known to be a very reliable and efficient low-bandgap absorber (Eg ~1.12 eV) [7], thermal losses limit its capacity to convert high-energy photons [8]. In order to address this, a tandem structure has been used, where a wide-bandgap cell at the front effectively converts the high-energy blue and visible light while silicon functions as the bottom cell to capture the red and near-infrared spectrum.

Cadmium Telluride (CdTe) is a highly desirable alternative for this front-cell position due to its recognized industrial stability and simple phase diagram, which allow for efficient thin-film production [9]. In contrast to newly developed organic or perovskite materials, CdTe has been commercially optimized for decades, yielding efficiencies in single-junction structures that exceed 23% [10]. However, the typical cell structure must be fundamentally redesigned in order to incorporate CdTe into a tandem device with silicon. In particular, the CdTe top cell needs to be fabricated as a bifacial device in order provide optical transparency for the bottom cell as well as collect albedo light.

The CdTe as a front cell act as a spectral filter in this specific tandem configuration [2]. As a top-junction solar cell, the CdTe front cell transfers lower-energy (infrared) photons to the bottom cell while absorbing higher-energy (visible) photons. In comparison to single-junction cells, this spectral filtering lowers thermalization losses, enabling a greater overall device efficiency (up to ~28–30%) [3].

A Transparent Back Contact (TBC), such as Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO), must be used instead of the conventional opaque back contact, which normally involves a metal stack, for best results. In order to perform as a bifacial solar cell, the CdTe absorber thickness must frequently be reduced to less than 1µm with a semi-transparent back contact to balance high-energy absorption and maximal transmission of sub-bandgap photons (<1.5 eV) to the silicon bottom cell. We previously investigated the reduction of absorber thickness [11]; in this work, we will replace the opaque back contact with a semi-transparent back contact to see how a bifacial CdTe top cell can be tuned to work with a silicon bottom cell in order to achieve a high-reliability, high-efficiency tandem photovoltaics device.

Bandgap selection has a direct impact on the efficiency of a tandem device. The Shockley-Queisser analysis determines an ideal top cell bandgap of roughly 1.70–1.75 eV for a bottom cell fixed at the silicon bandgap of 1.12 eV in order to achieve current matching in a series-connected (2T) device.

The bandgap of polycrystalline CdTe is around 1.5 eV. This is too thin for an ideal 2T tandem using silicon, despite being excellent for single-junction performance. A 1.5 eV top cell absorbs too much of the solar spectrum, resulting in a high current density that the silicon bottom cell cannot match due to insufficient photon flux [2]. The lowest-performing sub-cell (the silicon) in a series circuit limits the total current, significantly reducing the capacity of the top cell.

In a four-terminal configuration, the individual cells are electrically separated and connected by independent inverters. This eliminates the current matching limitation. According to simulations, even with a non-ideal 1.5 eV top cell, a CdTe/Si 4T tandem can achieve efficiencies above 30% if the top cell is highly transparent to sub-bandgap NIR light. Regardless of the current output of the top cell, the silicon cell can function at its maximum power point (MPP) because to the 4T configuration [2].

In this study, bifacial refers to two different yet connected optical characteristics. The CdTe top cell must be bifacial, meaning it has transparent connections on both the front and back sides, which enable sub-bandgap light (>850 nm) to pass through to the bottom cell.

The purpose of the complete tandem module is to collect albedo, or ground-reflected light. The silicon bottom cell can absorb light coming in from the back of the module because it is usually a bifacial PERC or HJT device [12], [13]. In 2T tandems, the extra current produced by the silicon cell from albedo can assist close the current mismatch gap brought on by the opaque CdTe top cell, making this rear-side illumination very useful.

According to research, under realistic field conditions with an albedo of 0.2-0.5 (e.g., fresh snow, dry grass surface, concrete or white sand), the bifacial gain can enhance the energy yield of the

bottom silicon cell by 10-30%, considerably improving the total energy equivalent efficiency of the tandem systems [13].

Lattice mismatch is a fundamental physical obstacle to monolithic (2T) CdTe/Si tandems. There is a 19% discrepancy between the diamond cubic lattice constant of silicon (5.43 Å) and the zincblende lattice constant of CdTe (6.48 Å)[14]. At the interface, a large density of threading dislocations (>10^8 cm^2) is produced via direct epitaxial growth of CdTe on Si [14]. These flaws spread throughout the absorber, serving as non-radiative recombination sites that significantly reduce the fill factor (FF) and open-circuit voltage (Voc). CdTe has a significantly higher coefficient of thermal expansion (CTE) (5.5–6.0) ×$10^{-6}K^{-1}$ than silicon (2.6×10^{-6} K^{-1}) at room temperature [15], [16], [17]. High-temperature deposition (over 500 ^oC) followed by cooling causes high tensile stress, resulting in cracking or delamination. The 4-terminal mechanically stacked structure, in which the two cells are constructed on different substrates and optically connected, is greatly favored by these physical limitations and completely avoids the epitaxial growth issues.

12.1.2 The Wide-Bandgap Top Cell

In order to optimize CdTe for tandem applications, the integration of selenium to form cadmium selenium telluride (CdSeTe) emerged as an essential materials engineering approach [18], [19]. Although early studies investigated into alloying with magnesium (CdMgTe) or zinc (CdZnTe) to increase the bandgap, these materials have significant instability and phase segregation [20]. In contrast, despite its novel effect on the bandgap, CdSeTe has been shown to be the key to achieving good performance in current CdTe devices.

As mentioned before. when CdTe (1.5 eV) and CdSe (1.7 eV) are alloyed, the bandgap of the resulting $CdSe_xTe_{1-x}$ alloy drops to about 1.4 eV [21], a phenomenon called optical band bending.

A broader bandgap (>1.6 eV) is usually preferred for a tandem top cell in order to optimize voltage and provide more light to the bottom cell. However, this lower-bandgap CdSeTe is used in the industry standard (as well as the methodology used in high-efficiency research).

The advantages of selenium in passivating defects and increasing carrier lifetime [19] much overcome the optical disadvantage of a slightly narrower bandgap. The excellent voltage performance of the CdSeTe absorber is more significant than a slightly higher transmission window in a 4-terminal setup when current matching is not necessary.

The CdSeTe layer's main function is to make it more effective electronic material than pure CdTe. Grain boundaries and intragrain imperfections that normally function as non-radiative recombination centers in polycrystalline CdTe are successfully passivated by selenium alloying [22]. According to literature, adding Se increase the minority carrier lifetime [19] from a few nanoseconds to more than 200 ns, which is a threshold for having open-circuit voltages (Voc) higher than 850 mV.

A graded $CdSe_xTe_{1-x}$ layer is formed at the front interface in an advanced device configuration, where the absorber is not uniform and gradually transitioning to pure CdTe in the back. This gradient generates an electric field that helps with carrier collection and moves the active junction away from the defective front interface.

The CdSeTe absorber must be optimized to balance transparency and absorption (current generation) for the particular use of a semitransparent top cell.

Recent experiments have shown that the absorber thickness may be drastically decreased to <1 µm (e.g., 800 nm) while keeping high structural quality by fine-tuning the CdSeTe/CdTe junction [11], [18]. This sub-micron thickness is necessary for sub-bandgap photons (up to 1.5 eV) to reach the silicon bottom cell.

The improved microstructure of the CdSeTe layer allows the use of a thinner absorber without the risk of pinholes or voltage collapse (shunting), which would be typical for pure CdTe films of the same thickness, even though the layer absorbs photons down to ~1.4 eV (about 885 nm). This maximizes the transmission of near-infrared light for the silicon bottom cell while enabling the device function efficiently as a spectral filter, converting high-energy blue/green light.

12.1.3 Semitransparent Back Contacts (TBC)

The single most significant barrier for CdTe/Si tandems is the back contact of the top cell. In standard opaque CdTe cells, this is a metal stack (Cu/Au or Mo). For a tandem, this contact must be highly transparent to Near-Infrared (NIR) light (>850 nm) while maintaining a low-resistance Ohmic contact to p-CdTe.

P-CdTe has a very high ionization potential and work function (~ 5.7 eV) [23]. Most high-conductivity Transparent Conductive Oxides (TCOs) like Indium Tin Oxide (ITO) or Aluminum-doped Zinc Oxide (AZO) are n-type degenerate semiconductors with work functions of 4.5–4.8 eV [24], [25], [26].

When these two materials come into direct contact, the CdTe valence band at the interface experiences a significant downward band bending due to Fermi level equilibration. This creates a Schottky diode that is reverse-biased and prevents holes to collect from the device. In the current density-voltage (J-V) curve, this barrier appears as a rollover or S-shape, especially in the first quadrant. This distortion is a blocking contact that significantly reduces the Fill Factor (FF) and raises the cell's series resistance.

Interestingly, whereas the Schottky barrier is a fundamental characteristic of the material interface, its effect on device performance is substantially influenced by absorber thickness.

In ultrathin CdTe cells (e.g., <1), the depletion region from the main p-n junction may extend through the entire thickness of the absorber, potentially overlapping with the back contact

region. This fully depleted state facilitates carrier collection by field-assisted drift, allowing holes to effectively bypass the back contact barrier and assist in sweeping carriers out of the device before they recombine at the back barrier, thereby mitigating the S-shape distortion [11].

In thicker devices (>2), there is a quasi-neutral region between the depletion edge and the back contact. Carriers must rely on diffusion instead of drift in this resistant zone. As a result, holes build up at the back interface in the absence of a sufficiently conductive ohmic contact, thereby raising series resistance and decreasing the Fill Factor (FF).

To get high performance using a transparent ITO contact, the interface must be designed to allow hole tunneling, hence overcoming the Schottky barrier.

The formation of a tellurium-rich layer on the CdTe surface before ITO deposition is one of the best methods. Cadmium atoms are selectively removed by chemical etching (e.g., with Bromine-Methanol or Nitric-Phosphoric acid), leaving behind a thin, highly conductive elemental tellurium or Te-rich layer [27], [28]. This layer greatly reduces the Schottky barrier's width, enabling holes to tunnel through it instead of having to thermionically overcome it.

In this paper, we present the design and optimization of a bifacial CdTe solar cell with Indium Tin Oxide (ITO) as a transparent back contact. In order to optimize front-side efficiency while preserving sufficient transparency for tandem applications, we investigate the differences between back contact material (Au vs. ITO), effect of different ITO and Cu layer thickness on the device performance.

12.2 Device Fabrication

In our lab, we use a low substrate temperature technique to fabricate CdTe solar cells in superstrate configuration [29]. We use vacuum evaporation to deposit a CdSe layer and then a CdTe layer on a commercial glass substrate coated with FTO/TO (SnO_2: F/SnO_2), known as TEC 12D, while maintaining the substrate's temperature at 340 °C. A quartz crystal monitor is used to measure the film thickness during the deposition process. We created CdSe/CdTe with a 2 µm absorber thickness.

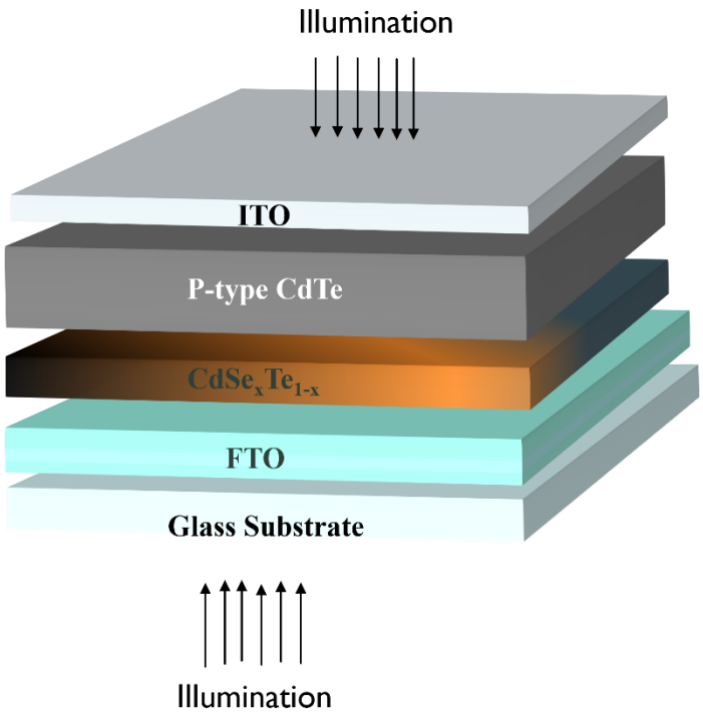

Figure 12.5 Sketch of the configuration of the semi-transparent devices fabricated and analyzed

The activation treatment is then applied by annealing in air at 390℃ after drop-casting a $CdCl_2$-methanol solution on the surface. In order to produce a desired $CdSe_xTe_{1-x}$ compound toward the junction, the $CdCl_2$ treatment additionally mixes the CdSe/CdTe layers [21]. In order to improve cell stability, the samples are further etched in a Br-MeOH solution, which simultaneously eliminates the $CdCl_2$ residuals from the surface and creates a Te-rich surface that encourages the synthesis of CuxTe at the CdTe/back contact junction [27], [28]. Copper is deposited at room temperature with a thickness of 1 & 2nm using vacuum evaporation.

Following this Indium Tin Oxide (ITO) was deposited by using RF sputtering to form the transparent back contact (Fig.12.1) at 200 ^{o}C temperature for 5 & 10 minutes. Finally, the sample undergoes an air annealing at 200 °C to diffuse Cu into the absorber.

12.2.1 Characterization

The current density-voltage (J-V) characteristics were measured under standard test conditions (AM 1.5G) for both front and back illumination. Optical transmission measurements were used to calculate the optical bandgap using Tauc plots.

12.3 Results and Discussion

To ensure that the top cell absorbs the appropriate portion of the solar spectrum, the optical bandgap was calculated from Tauc plot equation

$$(\alpha h\nu)^{\frac{1}{\gamma}} = A(h\nu - E_g) \qquad 12.1$$

The analysis confirms an optical bandgap of 1.4 eV as shown in figure 12.2. This value is consistent with modeling requirements for high-efficiency tandems, where a top cell bandgap of 1.4 eV can theoretically support tandem efficiencies exceeding 30% [30] when operated independently from the bottom cell.

A critical requirement for the top cell is that the transparent back contact must not degrade electrical performance compared to opaque standards. We compared the Jv analysis of a standard Au back contact to those with an ITO back contact (10-minute deposition).

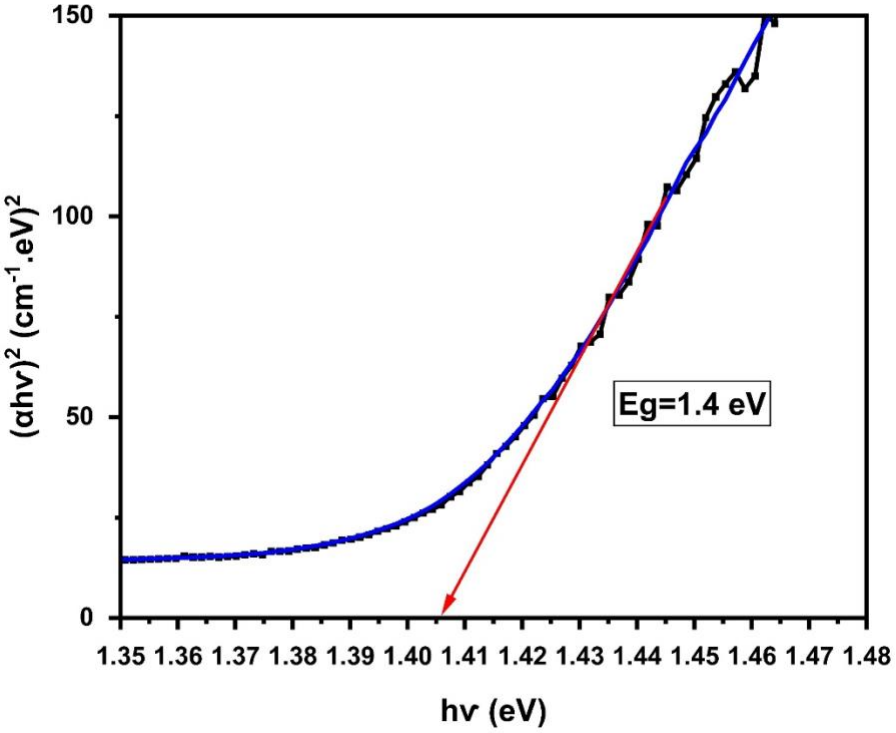

Figure 12.2: Optical band gap calculation (Tauc's plot) of the device having Thicker (10 minutes) ITO Layer

Au device achieved a best efficiency of 10.5% with a Voc of 720 mV and Jsc of 24 (mA/cm^2) where the ITO device achieved a comparable best efficiency of 10.2% with a Voc of 720 mV and Jsc of 23 (mA/cm^2) as shown in table-I. The J-V curves show (figure 12.3) nearly identical performance for front-side illumination, demonstrating that ITO can effectively replace Au (in case of our

reference sample) as the back electrode without compromising the primary junction performance. This is a crucial validation for the feasibility of semitransparent CdTe top cells.

Table 12.I - Peak and average efficiency parameters of samples fabricated with different Back contacts

Sample		Efficiency (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
Gold (Au)	Avg	10±0.2	58±0.5	711±3	24±0.3
	Best	10.5	60	720	24
ITO	Avg	10.2±0.1	62±0.6	727±2	22±0.2
	Best	10.2	60	720	23

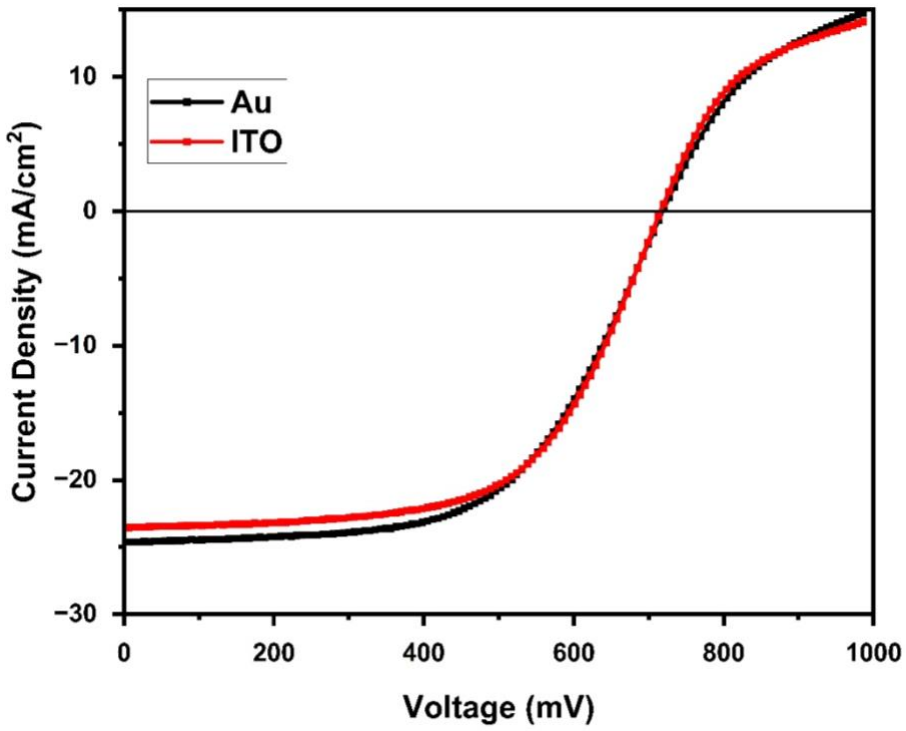

Figure 12.3: JV-curves of the samples fabricated with Gold (Au) and Copper (Cu) as back contact.

We further investigated the impact of ITO thickness on device performance. Two deposition times 5 and 10 minutes were tested assuming to have thinner and thicker layer of ITO film. Thicker ITO layer (10 minutes) resulted in an average efficiency of 10.2 ± 0.1% where the thinner layer (5 minutes) resulted in a lower average efficiency of 8.7 ± 0.2%. The thicker ITO layer yielded superior current collection and fill factor as compared to the tinner ITO layer having Jsc of 22 mA/cm^2 and 21.2 mA/cm^2 and fill factor 62% and 57%.

Table 12.II - Peak and average efficiency parameters of samples fabricated with different ITO Thickness

Sample		Efficiency (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
Thinner Layer (5 minutes)	Avg	8.7±0.2	57±0.2	718±4.6	21±0.5
	Best	9.35	57	727	22
Thicker Layer (10 minutes)	Avg	10.2±0.1	62±0.6	727±2	22±0.2
	Best	10.2	60	720	23

The thinner film offers higher optical transmission in the near-infrared region (approx. 50%) at 1000 nm where the thicker one shows only 35% transmission at the corresponding wavelength (figure 12.4). The electrical losses due to likely higher sheet resistance or poor coverage outweighed the optical benefits for the top cell itself.

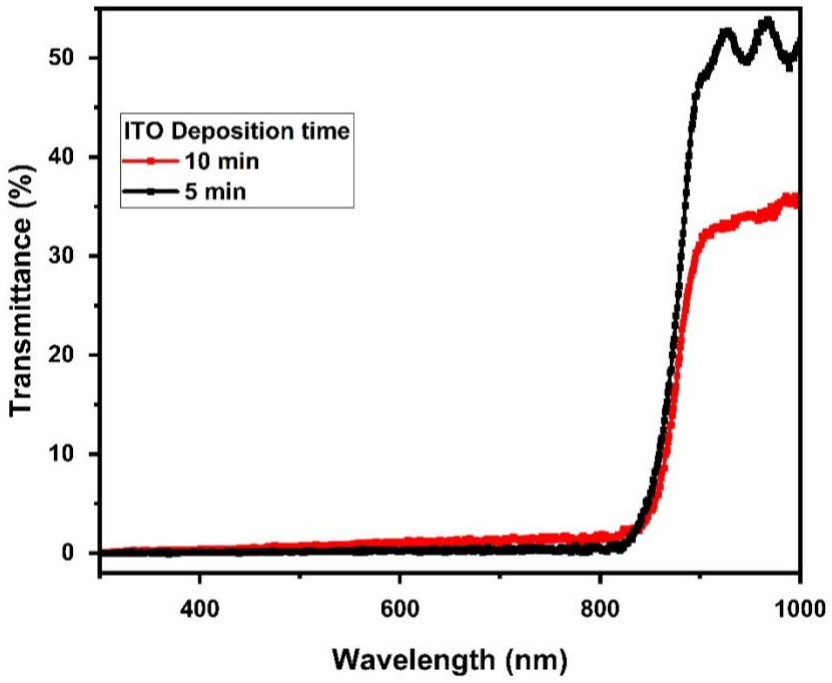

Figure 12.4: Graph of transmittance (T%) vs. wavelength for Thinner (5 minutes) and Thicker (10 minutes) ITO Layers

The thickness of the Cu buffer layer at the back interface is critical for forming an ohmic contact but can induce shunting or recombination if too thick. We compared 1 nm and 2 nm Cu layers. Thinner layer of copper (1nm) yielded an efficiency of 10.2%. where having thicker layer of copper

(2nm) Significantly lower performance to 7.2% efficiency. The degradation in the 2 nm sample was driven by a drastic drop in Fill Factor (54%) and Jsc, suggesting that excess copper may be diffusing into the absorber or creating shunt pathways. The optimized device having 1 nm copper with the 10 minutes deposition of ITO performed as a true bifacial cell. Under front illumination, the device reached 10.2% efficiency. Under back illumination, the device achieved 2.56% efficiency. The lower back-side efficiency is expected due to the absorption of high-energy photons in the thick (2 µm) CdTe layer before they reach the p-n junction located near the front interface. However, the high transparency on set near 850 nm confirms that the device is transparent to the sub-bandgap light required for a silicon bottom cell.

Table 12.III - Peak and average efficiency parameters of samples fabricated with different copper (Cu) Thickness

Sample		Efficiency (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
1 nm Cu	Avg	10.2±0.1	62±0.6	727±2	22±0.2
	Best	10.2	60	720	23
2 nm Cu	Avg	7.2	54	678	17
	Best	6.8±0.1	55±0.1	680±1.1	18.2±0.4

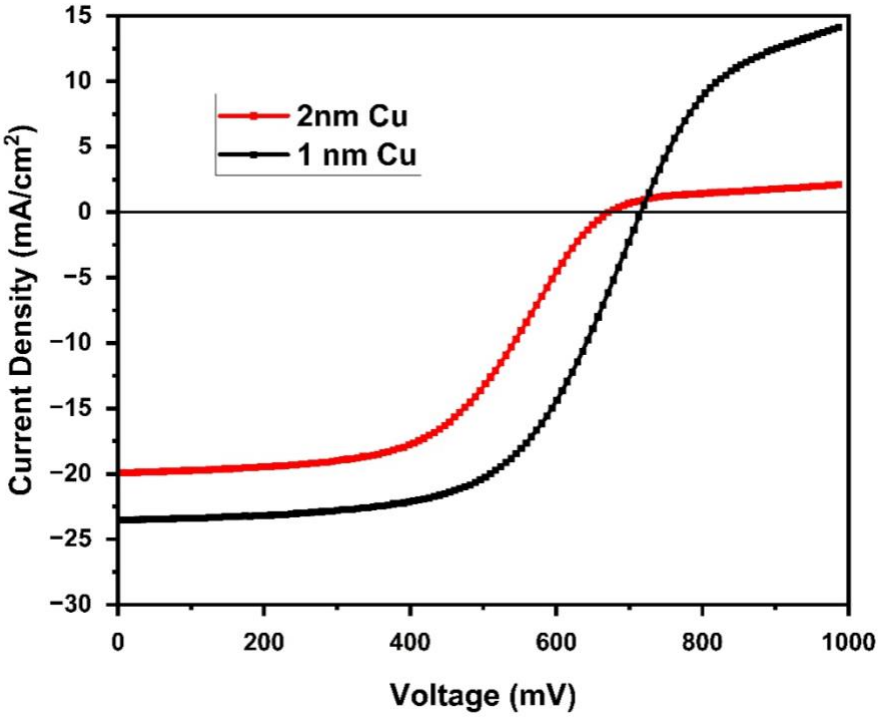

Figure 12.5: JV-curves of the samples fabricated with different Copper (Cu) Thickness

To evaluate the bifacial behavior of the optimized device (1 nm Cu / 10 min ITO), J-V measurements were conducted under rear-side illumination. The performance parameters for front and rear illumination are compared in Table 12. IV. Under standard front illumination, the device exhibited Jsc of 23~mA/cm^2 and an efficiency of 10.2%. However, under rear illumination (light entering through the ITO contact), the device achieved a Jsc of 6~mA/cm^2, a Voc of 615~mV, and an overall efficiency of 2.56%.

Table 12. IV - Peak and average efficiency parameters of the bifacial device from Front and Back illumination.

Sample		Efficiency (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
Front side Illumination	Avg	10.2±0.1	62±0.6	727±2	22±0.2
	Best	10.2	60	720	23
Rear side Illumination	Avg	2.5±0.2	62±2	608±3.5	6±0.2
	Best	2.56	64	615	6

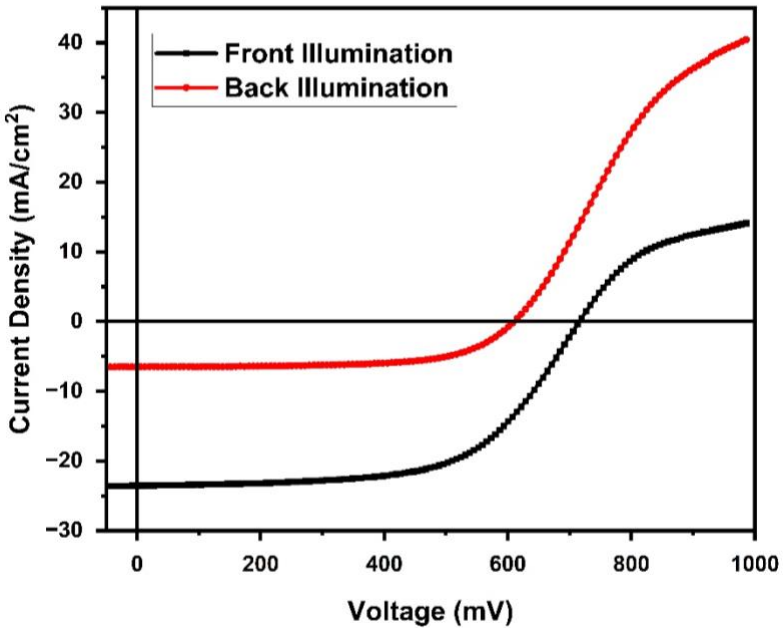

Figure 12.6: JV-curves of the bifacial device from front and back illumination.

The significant reduction in Jsc (from 23 to 6 mA/cm^2) under rear illumination is expected due to the device configuration. The p-n junction between CdTe and CdSe is placed at the front interface. High-energy photons (blue and green) are absorbed in the first few hundred nanometers of the

CdTe layer close to the back contact when light enters from the back. The carriers generated near the back surface recombine before reaching the junction at the front, failing to contribute to the photocurrent because the absorber thickness (~2μm) is greater than the average minority carrier diffusion length in polycrystalline CdTe.

As a result, longer-wavelength photons (red and near-infrared) that are deep enough to reach the depletion region are the main source of the current produced under rear illumination. This indicates that the ITO back contact is transparent enough to let light to enter the absorber, even while it reduces its rear-side efficiency. Additionally, the ITO/Cu contact maintains good carrier extraction capabilities independent of the direction of illumination, as seen by the maintenance of a high Fill Factor (64%) under rear illumination.

12.4 Conclusion

In this study, we successfully fabricate the semitransparent bifacial CdTe solar cell for mechanically stacked CdTe/Si tandem applications. By replacing the conventional metal rear contact with sputtered ITO, we were able to achieve a device efficiency of 10.2%. This result demonstrates that ITO can effectively function as a rear electrode without compromising the primary junction's functionality. Thicker ITO layer (10-minute deposition) shows higher fill factors and current collection, resulting in 10.2% efficiency as compared to the 8.7% for the thinner layer (5-minute). The thinner layer of ITO shows better optical transmission (50% at 1000 nm vs. 35%) than the thicker layer. The electrical losses for thinner ITO layers from higher resistance or inadequate coverage offset the optical benefits. It was essential to optimize the copper layer, a 1 nm layer was optimal as increasing the Cu thickness to 2 nm caused a significant drop in fill factor (to 54%) and total efficiency (to 7.2%), most likely due to copper diffusion.

The device bi-faciality was confirmed by the analysis, which produced 2.56% efficiency in rear lighting. Despite the limited rear-side current (6 mA/cm2), the device maintained a high Fill Factor of 64%, indicating that the ITO/Cu contact maintains good ohmic properties independent of the direction of illumination. Because of the 2 μm absorber thickness, high-energy photons absorbed close to the back contact recombine before they reach the front depletion region, which makes the decreased rear efficiency physically consistent with the device configuration. With an optical bandgap of 1.4 eV and transparency to sub-bandgap photons (>850 nm), the completed device satisfies the fundamental requirements for a top cell in a 4-terminal tandem arrangement. Future research will focus on optimizing the balance between ITO conductivity and transmission by reducing the absorber thickness to less than 1 μm in order to significantly increase the photon flux reaching the bottom silicon cell without lowering the electrical fill factor of the top cell.

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Chapter 13

Study of Sputtered ZnO Buffer Layers for CdSe/CdTe Solar Cells

13. 1. Introduction

This study investigates the optimization of Zinc Oxide (ZnO) buffer layers for cadmium selenide telluride (CdSeTe) solar cells with an absorber thickness of 2µm. We analyzed the effects of deposition temperature, oxygen concentration, and post-deposition vacuum annealing on device performance. Our results indicate that depositing ZnO at 400°C significantly improves optical transmittance, which is critical for thin absorbers. Contrary to expectations, increasing the oxygen flow rate during Radio Frequency (RF) sputtering reduced the shunt resistance (Rsh), likely due to plasma-induced damage. Furthermore, we identified an optimal vacuum annealing for 30 minutes at 450°C. The final device performance was stabilized using light soaking to eliminate metastable effects.

In this work, we focus on a specific device structure with a total absorber thickness of 2µm. In order to capture every possible photon at the front interface the buffer layer must be highly transparent. Zinc Oxide (ZnO) is chosen because ZnO has a wider bandgap (~3.3 eV), allowing more blue light to pass through to the absorber [1], [2]. However, depositing ZnO by RF sputtering introduces complex variables. We performed a series of experiments to study the effect of deposition temperature to maximize optical transmission, the effect of oxygen concentration during deposition to control the electrical resistance and the vacuum annealing of ZnO layer after deposition to improve the interface quality. The champion device, fabricated with a ZnO layer deposited at 300°C and 0.5 sscm oxygen flow, achieved a power conversion efficiency of 11%, demonstrating that moderate thermal budgets and balanced stoichiometry are critical for stabilizing the interface in thin-absorber photovoltaics.

13. 2. Device Fabrication

In our laboratory the solar cells were fabricated using a superstrate configuration. The ZnO buffer layers were deposited onto glass substrates using Radio Frequency (RF) magnetron sputtering. Following the CdSeTe absorber layer was deposited to a total thickness of 2µm.

ZnO films were deposited at substrate temperatures ranging from Room Temperature (RT) to 400°C. We measured the optical transmittance of these films to determine transparency. Based on optical results, devices were fabricated using deposition times of 5 and 10 minutes at 200°C, and 5 minutes at 400°C. We fixed the deposition time at 5 minutes and varied the oxygen flow rate during sputtering at 0.3 sscm, 0.5 sscm, and 1.0 sscm. A post-deposition vacuum annealing step was introduced after ZnO deposition at 450°C for durations of 15, 30, and 45 minutes.

13.3. Results and Discussion

Our initial experiment measured the transmittance of ZnO layers deposited from 200°C up to 400°C. The results show at a 200 °C deposition temperature, thinner ZnO layers (5 min) exhibited optical behavior similar to reference cells (FTO), while thicker layers (10 and 20 min) showed significant optical losses. As deposition temperature and thickness increased, optical losses at shorter wavelengths became more evident as shown in figure 13.1.

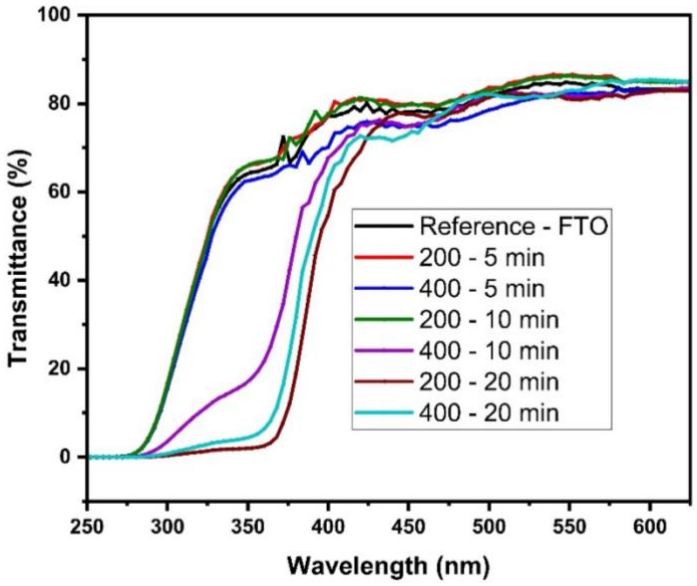

Figure 63.1: Transmittance of glass/FTO/ZnO with different deposition time and substrate temperature.

The reduction in optical transmittance with increasing film thickness follows the Beer-Lambert relation [3]. This law states that the intensity of light transmitting through a material decreases exponentially with the thickness of that material[4]:

$$\boldsymbol{I = I_0 e^{-\alpha d}} \qquad (\mathbf{13.1})$$

Where I_0 is the incident light intensity α is the absorption coefficient of ZnO and d is the film thickness.

To further investigate the effect of oxygen, we varied the oxygen flow (0.3, 0.5, and 1 sscm) during sputtering. Interestingly, increasing the oxygen concentration resulted in a slight increase in short-circuit current (Jsc), rising from 23 mA/cm² at 0.3 sscm to 25 mA/cm² at higher flows.

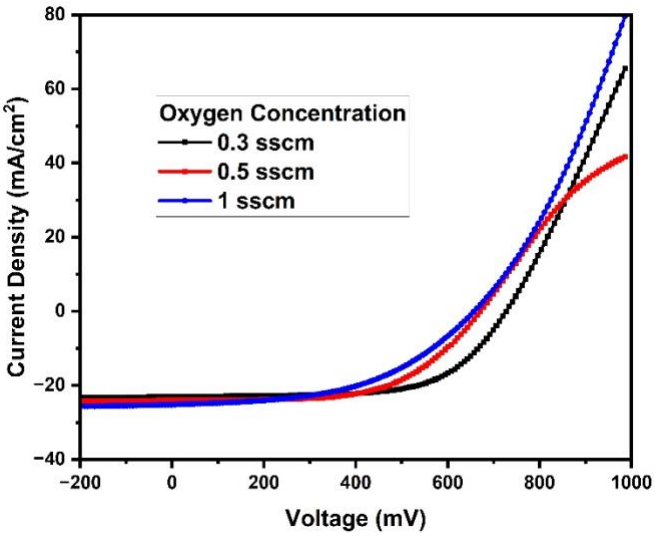

Figure 13.7: Jv analysis of different oxygen concentration during ZnO deposition

This can be attributed to improved stoichiometry, higher oxygen pressure reduces the density of oxygen vacancies, thereby decreasing free-carrier absorption and making the ZnO layer more transparent to incident light [5]. However, this optical gain was heavily outweighed by severe electrical losses. While the window became clearer, the structural integrity of the device was compromised. The high-energy oxygen ion bombardment created leakage paths (shunts) that drastically reduced the shunt resistance (Rsh). As seen in the J-V curves, the 0.5 and 1.0 sscm devices exhibit a significant slope near the short-circuit condition and a premature crossover at the voltage axis. Consequently, despite the higher current generation, the inability to maintain voltage (Voc) and fill factor (FF) led to a net decrease in overall efficiency. ZnO is naturally n-type due to oxygen vacancies. Adding oxygen fills these vacancies, altering the carrier concentration and optical properties [6]. Normally, adding oxygen makes ZnO more resistive, which should help block electrical shunts. However, in RF sputtering, oxygen forms negative ions (O^-) in the plasma [7], [8]. These ions are accelerated by the electric field and bombard the growing film on the substrate, a phenomenon known to induce structural defects and microscopic voids. These voids can act as leakage paths for the subsequent CdSeTe layer, leading to low R_{sh} and poor fill factor [7].

Table 13. I - Peak efficiency parameters of the different oxygen concentration Device.

Oxygen Concentration (sscm)	Eff (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
0.3	10.7	63	734	23
0.5	8.33	53	622	25
1	8.17	48	664	25

At 0.3 sscm (low oxygen) the bombardment is minimal, allowing a dense, continuous film to grow. At 1.0 sscm (high oxygen) the flux of high-energy oxygen ions increases. This bombardment acts like a sandblaster, creating microscopic voids, pinholes, or porosity in the film. These physical defects and pinholes allow current to leak through the buffer layer, drastically reducing the shunt resistance (Rsh) and degrading device performance [9].

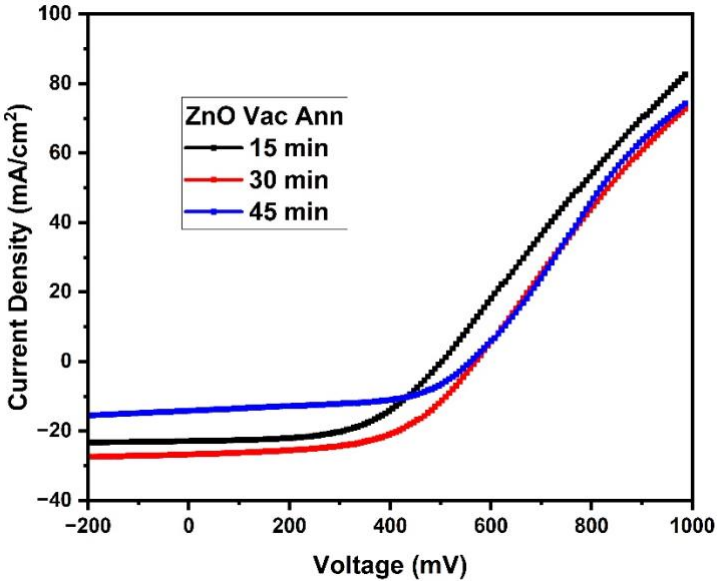

Figure 13.8: JV curves of vacuum anneal ZnO Device with different time duration

We introduced vacuum annealing at 450°C after ZnO deposition to improve the interface. We tested three-time durations 15 minutes which was insufficient to fully relax the lattice stress or activate the necessary electrical conductivity in the ZnO. 30 minutes treatment (optimal) provided the best balance. The heat treatment allowed the ZnO atoms to settle into lower-energy positions, reducing defects at the ZnO/CdSeTe interface. Vacuum annealing also creates oxygen vacancies (V_O), which are necessary to ensure that the ZnO is conductive enough to collect

electrons efficiently. However, if the treatment is extended to 45 minutes the performance of the finishes devices is degraded. Prolonged heating at 450°C likely caused interdiffusion, where elements from the glass (like sodium) diffuse into the buffer layer [10], [11], creating recombination centers that decrease the voltage [12], [13].

Table 13. II - Peak efficiency parameters of the Vacuum anneal ZnO Device.

Vacuum Annealing time (ZnO)	Eff (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
15 minutes	6.29	54	503	22
30 minutes	8.36	54	573	26
45 minutes	4.43	55	566	14

We also applied FTO annealing before the ZnO deposition but the devices without FTO annealing deliver a higher performance. In a vacuum, oxide materials like ZnO and SnO_2 (FTO) tend to lose oxygen atoms into the atmosphere at high temperatures [14].

$$\boldsymbol{O_o \rightarrow V_o + \frac{1}{2} O_2} \qquad (\mathbf{13.2})$$

This creates an excess of metal ions (zinc or tin). If too much oxygen is lost, microscopic metallic filaments can form. These filaments create direct conductive paths (shorts) through the buffer layer, connecting the front contact directly to the absorber affecting the open circuit voltage.

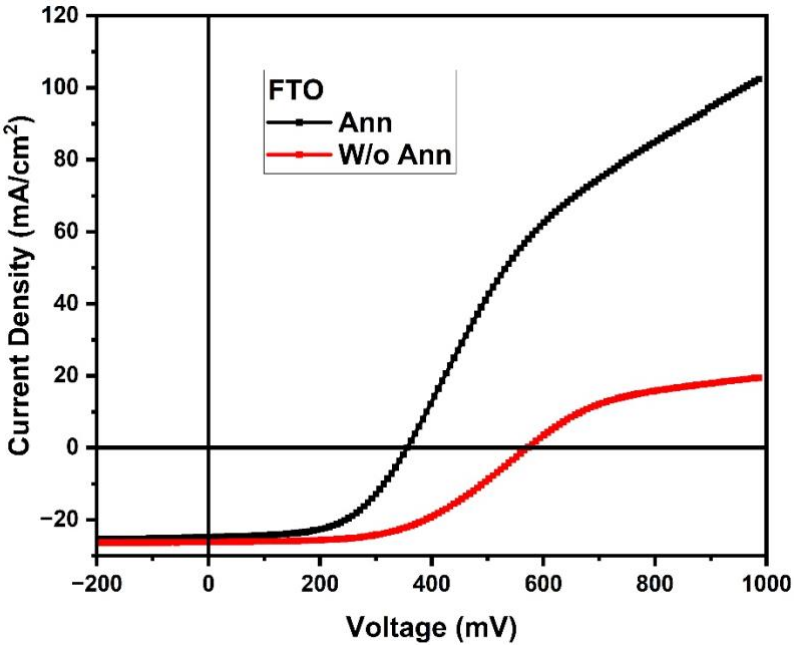

Figure 13.9: Jv analysis of device with and without FTO annealing at 450 °C

With a temperature of 450 °C, impurities like sodium (Na) from the soda-lime glass or tin (Sn) from the FTO layer gain enough thermal energy to diffuse through the thin ZnO layer and into the CdSeTe absorber. As a result, these impurities act as deep-level recombination centers.[13], trapping electrons and holes before they can be collected, delivering the massive drop in voltage shown in the black curve in figure 13.4.

Without annealing, (see red curve in figure 13.4) the layer is in a "metastable state" that can be affected by subsequent deposition steps but however avoids possible impurities and/or a secondary phase at the interface (e.g., zinc silicate or excessive oxidation of the CdSeTe surface if any residual oxygen was present) that can give place to the band misalignment.

Table 13. III - Peak efficiency parameters of the FTO with and without Annealing.

Vacuum Annealing (ZnO)	**Eff (%)**	**FF (%)**	**Voc (mV)**	**Jsc (mA/cm²)**
Ann	4.91	55	356	24
W/o Ann	7.85	52	573	26

To study the effect of temperature deposition, we deposit ZnO at different substrate temperature ranging from room temperature up to 400 degrees.

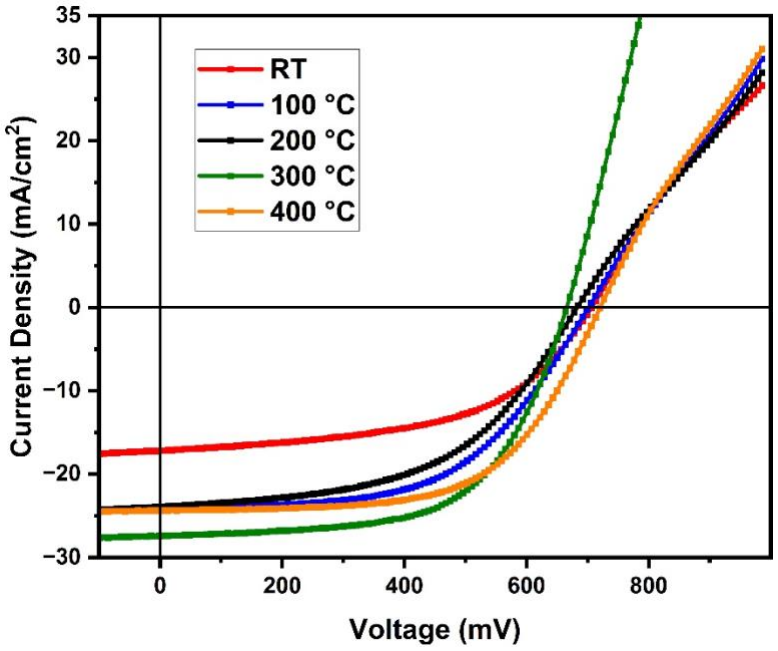

Figure 13.10: Jv analysis of device with different ZnO deposition temperature

As we increased the ZnO deposition temperature from room temperature (RT) to 300°C, the device performance steadily improved. At low temperatures, the ZnO film is nanocrystalline or amorphous with many grain boundaries. These boundaries scatter light, reducing the current (J_{sc}). As temperature rises to 300°C, the grains grow larger and columnar. This reduces scattering, allowing more photons to reach the CdSeTe absorber, which explains the massive jump in current from the red curve (~18 mA/cm²) to the green curve (~28 mA/cm²).

The higher Voc obtained with an annealing at 300°C suggests a reduction in interface state density. The 300°C deposition likely provided a cleaner, more chemically stable surface for the subsequent CdSeTe growth, reducing recombination centers at the junction.

Moreover, the performance drops when going from 300°C (green) to 400°C (orange). The orange curve has lower voltage and lower current than the green one.

At 400°C, the ZnO grains grow very large and competitive, creating a rough surface**.** For a 2µm thin absorber, this roughness is dangerous. Sharp peaks of ZnO can penetrate into the active region of the device, creating weak spots in the electric field where carriers recombine, lowering the Voc. The 400°C is high enough to trigger the diffusion of sodium (Na) from the glass substrate or tin (Sn) from the FTO into the ZnO and the absorber. These impurities act as deep-level defects, hurting performance.

13.4. Conclusion

This study investigates the deposition and post-processing conditions of sputtered Zinc Oxide (ZnO) buffer layers to enhance the performance of ZnO/CdSeTe solar cells. The investigation focused on the impact of film thickness, oxygen concentration during sputtering, deposition temperature, and annealing protocols on device parameters.

The optical characterization confirmed that transmittance losses in ZnO follow the Beer-Lambert relation, with thicker films (10–20 min deposition) showing significant optical losses at shorter wavelengths. Thinner layers deposited at 200°C were found to be optically superior, exhibiting transmittance behavior comparable to reference FTO substrates.

A critical and counter-intuitive finding was observed regarding oxygen flow during RF sputtering. Contrary to the expectation that increased oxygen would reduce vacancies and improve resistance, higher oxygen concentrations (1.0 sscm) severely degraded the shunt resistance (Rsh) and fill factor. This is attributed to the bombardment of the growing film by high-energy negative oxygen ions (O^-), which induce pinholes. Consequently, a low oxygen flow rate of 0.3 sscm was identified as optimal, yielding a dense, continuous film and a peak device efficiency of 10.7%.

Thermal profiling revealed distinct process windows for both deposition and annealing. The optimal substrate temperature for ZnO deposition was identified as 300°C. This temperature maximizes short-circuit current (Jsc~28 mA/cm²) which might be because of the growth of large, columnar grains that reduce grain boundary scattering. Lower temperatures resulted in poor crystallinity, while higher temperatures (400°C) caused surface roughness and detrimental impurity diffusion (Na, Sn) from the substrate, leading to a drop in open-circuit voltage (Voc).

Post-deposition vacuum annealing of the ZnO layer at 450°C for 30 minutes proved effective in relaxing lattice stress and improving the ZnO/CdSeTe interface. However, extending this time to 45 minutes degraded performance due to interdiffusion. Furthermore, pre-annealing the FTO substrate was found to be detrimental, as oxygen loss in the vacuum promoted the formation of metallic filaments and diffusion pathways, creating electrical shorts that drastically reduced cell efficiency.

In summary, the highest device performance is achieved by combining a 300°C deposition temperature with a low-oxygen sputtering environment (0.3 sscm) and a controlled 30-minute post-deposition anneal. These conditions effectively balance the difference between crystal quality, interface stability, and defect mitigation.

13.5. References

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Final Conclusion

This PhD thesis investigated the development of cadmium telluride (CdTe) photovoltaics from a conventional single-junction technology to a high-efficiency, sustainable, tandem construction. The initial study of absorber engineering revealed that CdSeTe/CdTe devices fabricated by evaporation, followed by vacuum annealing at 450 °C to mix CdSe and CdTe layers, is an important step to increase conversion efficiency. XRD, Raman, and SIMS investigations revealed that this thermal treatment increases Se-Te interdiffusion while reducing hazardous elemental tellurium at the surface. Selenium alloying increases minority carrier lifespan by reducing deep-level Te interstitials, which normally serve as lifetime-limiting recombination hubs. These improvements resulted in a record 14.7% efficiency for 2 µm thick devices manufactured at low substrate temperatures.

Based on these core results, the research successfully moves toward ultra-thin absorbers to reduce tellurium deficits and ensure RoHS compliance for indoor applications. Thanks to CdTe's high absorption coefficient (10^4 cm^{-1}) which allows to absorb more than 90% of light within ~1 µm thickness. Currently, in our laboratory, samples with a 0.8 µm thick absorber (which satisfies RoHS rules for consumer electronics) have reached efficiencies of 11 %, with good current densities of 25 mA/cm^2 and decent Voc and FF values. By further reducing the absorber thickness, all the efficiency parameters decrease. As expected, EQE shows the loss of carriers at long wavelengths for the thinner absorbers, explaining the lower current. On the other hand, CV-DLCP profiles indicate a higher presence of deep defects for the thinner absorbers. Moreover, these measurements suggest that in the 0.5 µm case, the absorber is completely depleted, favoring the recombination of the carriers near the back contact. This points out that to further reduce the thickness of the absorber, an electron reflector should be introduced.

It is now essential to understand the impact of selenium incorporation in ultra-thin CdTe absorbers. Interestingly, in thinner cells, there is no evidence of the CdSeTe/CdTe bi-layer structure observed as compared to the thicker CdTe. Selenium diffuses throughout the entire absorber, even using 75/725 nm of CdSe/ CdTe. With this ratio, SIMS analysis suggests the formation of a graded band gap, with a decreasing concentration of Se towards the back contact; even if the hyperspectral CL map shows that the band gap of the absorber mainly changes from grain to grain, thus also parallel to the substrate. By increasing the CdSe/CdTe ratio, the measurements show a progressive reduction of the minimum band gap and an increase in the net charge density, thus demonstrating the insertion of Se into the lattice structure and its function of passivation of the grain boundaries. Furthermore, enhancing the net charge density

narrows the depletion region width, a factor that should not be neglected given the thin absorber thickness; a completely depleted absorber leads to increased recombination in the back contact region. On the other hand, by increasing the selenium concentration, a progressive decrease in grain size occurs along the entire thickness of the absorber. It is, therefore, not limited to the junction region alone. This inevitably increases the amount of grain boundaries and, hence, the possible carrier recombination. Using a CdSe/CdTe ratio of 1/1, a structure composed of small, disorderly-arranged grains is formed, with also the presence of voiding. This results in a marked reduction in quantum efficiency for all wavelengths and, consequently, a drop in device performance. Selenium introduction also affects the stability of the devices: accelerated stability tests prove that by increasing Se concentration, the stability of the cells reduces, mainly due to the degradation of Voc. The 150/650 nm CdSe/CdTe samples fabricated without Br-MeOH etching demonstrate the best compromise between the effects of the selenium introduction mentioned above, leading to the highest performances. Currently, in our laboratory, these samples have reached a remarkable (considering the ultra-thin absorber) efficiency of 12.8 %. The different Se concentrations in different grains have been attributed to the energetically favorable diffusion of Se through specific crystal orientations of CdTe compared to others. In a 2–3 μ m thick as-deposited CdTe, a few layers of grains form the film thickness; thus, while diffusing through the grain boundaries, Se can surround the grains of the first layer/layers and enter through the preferred orientation into the matrix. On the other hand, if the grains extend throughout the entire thickness of the as-deposited CdTe, Se is disadvantaged during the activation treatment in accessing some grains, depending on their orientations. Moreover, starting from a CdTe film composed of a single layer of grains, it is impossible to obtain a CdSeTe/CdTe bi-layer; this limits the grain size growth throughout the absorber.

We further investigate the role of oxygen incorporation during the fabrication of CdSeTe absorber by close-spaced sublimation (CSS). Despite having much smaller grains (~0.5 μm vs. >1.7 μm), our results show that oxygen-exposed absorbers achieve superior device efficiency (12.9%) compared to their oxygen-free counterparts (9.1%), disregarding conventional assumptions that maximize grain size is the primary driver of performance. The ODX absorber performance is attributed to the segregation of oxygen to grain boundaries and interfaces, where it functions as an effective passivant. This mechanism reduces non radiative recombination and suppresses shunt pathways, leading to a marked improvement in open-circuit voltage (~660 mV) and shunt resistance. Conversely, the oxygen-free process, while having extensive grain growth, suffers from reduced voltage (~580 mV) and fill factor due to un passivated defects and the formation of voids driven by the differing sublimation rates of CdSe and CdTe. Ultimately, these findings highlight that microstructural size is secondary to electronic quality in CdSeTe absorbers. We conclude that controlling oxygen exposure during deposition is a vital lever for optimizing alloy composition and

defect management, offering a strategic pathway to enhance the stability and efficiency of next-generation CdSeTe thin-film solar cells.

Beyond microstructural passivation, the electronic properties were further enhanced through group V doping. We investigate the influence of ambient air atmosphere on the performance of 2µm thick arsenic-doped cadmium telluride (As: CdTe) solar cells. By comparing standard air activation with inert nitrogen processing, we demonstrated that the activation environment is the critical determinant for successfully leveraging Group V dopants. Our results indicate that standard air activation is incompatible with Arsenic doping, leading to dopant deactivation and a significant reduction in device performance (~14.35%). In contrast, activation in a nitrogen atmosphere successfully prevented dopant oxidation, unlocking the full potential of the Arsenic acceptor. The nitrogen-activated devices achieved a champion efficiency of 17.11%, effectively outperforming the intrinsic CdTe control (16.24%). This performance boost was driven by a concurrent increase in Open Circuit Voltage (Voc~850 mV) and Fill Factor (77.4%), supported by a doubling of the shunt resistance (>3300 $\Omega.cm^2$).Crucially, this study highlights a no-compromise regime for As-doped CdTe unlike literature reports where inert activation often degraded carrier collection, our optimized nitrogen process maintained a high short circuit current (Jsc~26 mA/cm^2) comparable to the air-activated CdTe cell. We conclude that inert atmosphere activation is essential for realizing high-efficiency, As-doped CdTe photovoltaics, providing a viable pathway to exceed the performance limits of standard copper-doped technologies.

Finally, the integration of these advanced absorbers into a bifacial structure demonstrated a scalable pathway for 4-terminal CdTe/Silicon tandem applications. We successfully fabricate the semitransparent bifacial CdTe solar cell by replacing the conventional metal rear contact with sputtered ITO, we were able to achieve a device efficiency of 10.2%. This result demonstrates that ITO can effectively function as a rear electrode without compromising the primary junction's functionality. Thicker ITO layer (10-minute deposition) shows higher fill factors and current collection, resulting in 10.2% efficiency as compared to the 8.7% for the thinner layer (5-minute). The thinner layer of ITO shows better optical transmission (50% at 1000 nm vs. 35%) than the thicker layer. The electrical losses for thinner ITO layers from higher resistance or inadequate coverage offset the optical benefits. It was essential to optimize the copper layer, a 1 nm layer was optimal as increasing the Cu thickness to 2 nm caused a significant drop in fill factor (to 54%) and total efficiency (to 7.2%), most likely due to copper diffusion. The device bi-faciality was confirmed by the analysis, which produced 2.56% efficiency in rear lighting. Despite the limited rear-side current (6 mA/cm2), the device maintained a high Fill Factor of 64%, indicating that the ITO/Cu contact maintains good ohmic properties independent of the direction of illumination. Because of the 2 µm absorber thickness, high-energy photons absorbed close to the back contact recombine before they reach the front depletion region, which makes the decreased rear efficiency physically consistent with the device configuration. With an optical bandgap of 1.4 eV

and transparency to sub-bandgap photons (>850 nm), the completed device satisfies the fundamental requirements for a top cell in a 4-terminal tandem arrangement.

Collectively, the strategies presented in this thesis spanning from selenium incorporation, absorber engineering and ultra-thinning to transparent contact optimization, CdTe can be successfully integrated into tandem configurations with silicon. This approach provides a strategic route to cross the Shockley-Queisser limit, utilizing a combination of stable, commercially established materials to drive the future of thin-film photovoltaics.